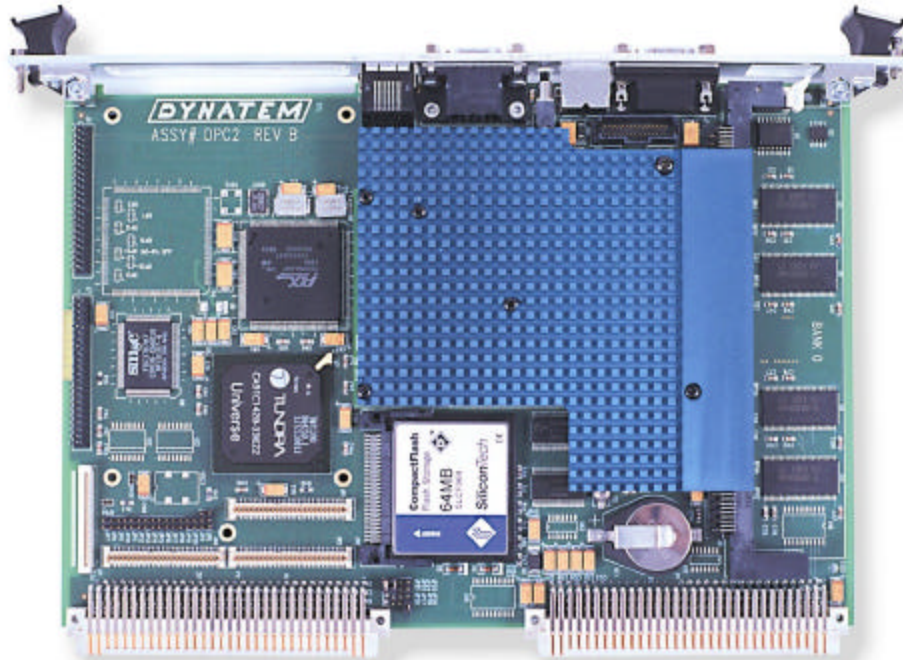




## DPC2 VMEbus Pentium III Processor Board User's Manual



DPC2 User's Manual Rev. 1.02

October 2001

**Note:** This user's manual uses jumper designators that only apply to DPC2 boards of revision D or greater. To determine the module's revision, it will be printed below the "DYNATEM" logo near the front panel opening for the module's PMC expansion card.

Revisions to Rev. 1.02:

There is a minor correction on page 1 (a reference to an RJ45 connector was removed).

2 MB of SRAM are featured in the block diagram on page 5 (instead of the incorrect 1 MB).

The correct timeout period of 1.2 seconds for the watchdog was added to page 19.

JP30 (on DPC2 Rev D and beyond) is now listed on page 26.

+/- 12 VDC was removed from the power spec's on page 46 (neither supply is needed).

## **Dynatem**

23263 Madero, Suite C

Mission Viejo, CA 92691

Phone: (949) 855-3235

Fax: (949) 770-3481

[www.dynatem.com](http://www.dynatem.com)

# Table of Contents

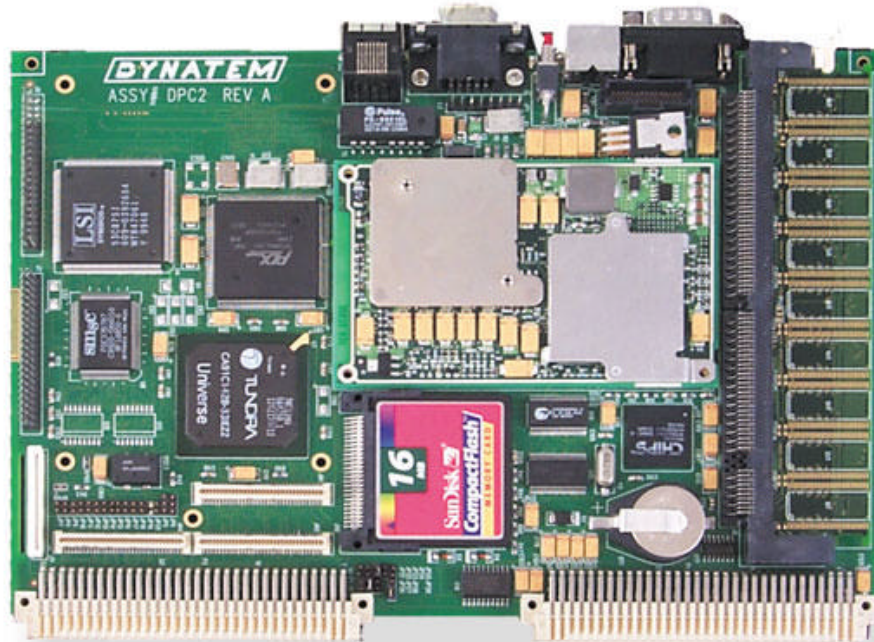
<b>1.</b>	<b>Features</b>	<b>1</b>
<b>2.</b>	<b>Related Documents</b>	<b>3</b>
<b>3.</b>	<b>Hardware Description</b>	<b>5</b>
3.1	Overview	5
3.2	Pentium III Processor	6
3.3	Intel 82443BX Chipset	6
3.4	DRAM	6
3.5	Asiliant 69030 HiQVideo Accelerator with 4 MB SDRAM	7
3.6	Symbios SYM53C875 Ultra Wide SCSI Controller	7
3.7	Intel 82559 Fast Ethernet Controller	8
3.8	Tundra Universe IIB CA91C142B PCI-VMEbus Interface	9
3.9	PCI Mezzanine Card (PMC) Slot	12
3.10	PLX PCI9050-1 PCI Interface For Dual Port Memory	13
3.10.1	Big/Little Endian Translation	13
3.10.2	Preventing PCI/VMEbus Contention	14
3.11	SMSC FDC37B78x Multi I/O Controller	15
3.12	Real Time Clock and NVRAM	16
3.13	Intel 28F008B3 System BIOS Flash Memory	16
3.14	Clock Drivers	17
3.15	Reset Circuitry	18
3.16	Watchdog Timer Operation	19
3.17	Interrupt Logic	21
<b>4.</b>	<b>Installation</b>	<b>23</b>
4.1	Jumper Selectable Options	25
4.2	CompactFlash Drive Installation	28
4.3	PCI Mezzanine Card (PMC) Installation	28
4.4	VMEbus Chassis Installation	29
4.5	Front Panel Connections	29
4.6	Front Panel Reset Switch and LEDs	29

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<b>A.</b>	<b>Connector Pin-outs</b>	<b>31</b>
A.1	PS/2 Keyboard/Mouse Connector (J1)	32
A.2	JTAG Debug Port (J6)	32
A.3	10BaseT/100BaseTX Fast Ethernet Connector (J4)	33
A.4	VGA Connector (J2)	33
A.5	COM1 Connector (J3)	34
A.6	Primary IDE Interface Connector (J7)	34
A.7	CompactFlash Interface Connector (J10)	35
A.8	Floppy Drive Interface Connector (J11)	36
A.9	PCI Mezzanine Card (PMC) Connectors (JN1 and JN2)	37
A.10	VMEbus Connectors (P1 and P2)	39
A.11	External BIOS and USB Connector Pin-out (J5)	42
<b>B.</b>	<b>Address Maps, Interrupts, DMA Channels</b>	<b>43</b>
B.1	Memory Map	43
B.2	PCI/AGP Configuration Space Map	43
B.3	Interrupt Request Routing	44
B.4	ISA DMA Channel Assignments	45
B.5	PCI Bus Request/Grant Routing	45
<b>C.</b>	<b>Power and Environmental Requirements</b>	<b>46</b>

## 1. Features

The Dynatem DPC2 is a single-slot 6U VMEbus Single Board Computer (SBC) that combines the power, versatility and cost-effectiveness of the Pentium-based PC architecture with the reliability and ruggedness of the VMEbus form factor.



The DPC2 uses Intel's cool running version of the Embedded Module Connector-2 (EMC-2) known as the Low Power Module (LPM). The LPM supports a Pentium III processor and on-die L2 cache as well as PCI, AGP, and DRAM interfaces. The optional absence of socketed components also contributes to the module's ruggedness.

Features of the DPC2 include:

- Single-slot VMEbus operation with on-board CompactFlash disk for bootable mass storage and front panel connectors for Keyboard/Mouse, COM1, VGA, 10/100BaseTX, and a PCI Mezzanine Card (PMC).
- SCSI, COM2, LPT1, PMC I/O and, optionally, IDE and FDC are routed out a five-row VME64 P2 connector.
- Supports Intel's EMC-2 Low Power Module (LPM) which supports a Pentium III with on-die cache.
- High-performance Intel BX chipset (Northbridge component is on the LPM) with DRAM controller, PCI bus arbitration logic and interface, AGP graphics interface, high performance PCI IDE interface, RTC, NV-RAM, standard PC timers, Ultra DMA, and interrupt logic.

## Chapter 1 – Features

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- Supports on-board SDRAM of up to 128 MB. DIMM module for additional 3.3V PC100 SDRAM memory of up to 256 MB. In total, 384 MB of SDRAM may be supported.
- Tundra Universe IIB PCI-VMEbus Interface provides 64-bit VMEbus transfer rates over 30 MB/sec. Integral FIFOs permit write-posting to maximize available PCI and VMEbus bandwidth. Full Slot 1 (System Controller) functionality is provided.
- Asilant's 69030 AGP-compatible graphics controller with 4 MB of SDRAM built-in to the chip.
- Symbios' 53C875 Ultra SCSI Controller with data transfer rates up to 40 MB/sec.
- Intel's 82559 Fast Ethernet Controller with 10/100BaseTX support.
- On-board auxiliary memory includes 2 MB of SRAM, which can be accessed from the VMEbus or the on-board Pentium III without byte-swapping or bus contention issues, and up to 8 MB of flash space.
- PCI Mezzanine Card (PMC) support with front panel I/O, while maintaining VMEbus single-slot form factor.
- Primary Ultra DMA IDE Interface with improved transfer rates and PIO and Bus Master support.
- Secondary IDE port for CompactFlash on-board booting for flash-based and mechanical storage.
- General Software's flash-based system BIOS that's upgradeable via floppy.
- Floppy drive controller with support for drives of up to 2.88 MB.
- COM1 and COM2 serial ports, based on 16C550 compatible UARTs with 16-byte transmit and receive FIFOs. Either port can be configured for RS-232 or RS-422/485 operation.
- LPT1 parallel port that's capable of standard, bidirectional, enhanced parallel port (EPP), and enhanced capabilities port (ECP) operation, with IEEE 1284 compliance.
- Programmable watchdog timer for system recovery.
- Operating System (OS) and driver support, including Windows NT, Embedded NT, QNX, VxWorks, Linux, Solaris, and pSOS+.

## 2. Related Documents

Listed below are documents that describe the Pentium processor and chipset, and the peripheral components used on the DPC2. Contact your local distributor for copies of these documents.

For a data sheet on the EMC-2 LPM, go to:

**<http://developer.intel.com/design/intarch/prodbref/273193.htm>**

For Intel data, go to:

**<http://developer.intel.com/design/litcentr/index.htm>**

The Intel website is subject to change but the following documents should be available and downloadable:

- *Pentium Processors and Related Products*  
Intel Corporation
- *Intel 440BX AGPset – 82443BX Host Bridge/Controller*  
Intel Corporation, Document Number 290633-001
- *Intel 82371AB PCI-TO-ISA / IDE Xcelerator (PIIX4)*  
Intel Corporation, Document Number 290562-001
- *Intel 82371EB (PIIX4E) Specification Update*  
Intel Corporation, Document Number 290635-008
- *82559 Fast Ethernet Multifunction PCI/CardBus Controller*  
Intel Corporation, Document Number 743892-002
- *69030 Data Book*  
Asilient Technologies
- *SYM53C875 Data Manual*  
Symbios Logic
- *VMEbus Interface Components Manual*  
Tundra Semiconductor Corporation; Universe IIB revisions are found at [www.tundra.com](http://www.tundra.com)
- *FDC37B78X Data Sheet*  
Standard Microsystems Corporation

## Chapter 2 – Related Documents

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The following documents provide information on the PC architecture:

- *PCI Local Bus Specification, Revision 2.1*  
PCI Special Interest Group
- Hans-Peter Messmer, *The Indispensable PC Hardware Book*  
Addison-Wesley
- Frank van Gilluwe, *The Undocumented PC*  
Addison-Wesley

The following documents cover topics relevant to the VMEbus and can be purchased through VITA:

- IEEE Std 1014-1987, *IEEE Standard for a Versatile Backplane Bus: VMEbus*  
The Institute of Electrical and Electronic Engineers  
345 East 47th Street  
New York, NY 10017  
(800) 678-4333
- Wade D. Peterson, *The VMEbus Handbook*  
VITA  
10229 North Scottsdale Road, Suite B  
Scottsdale, AZ 85253  
(480) 951-8866

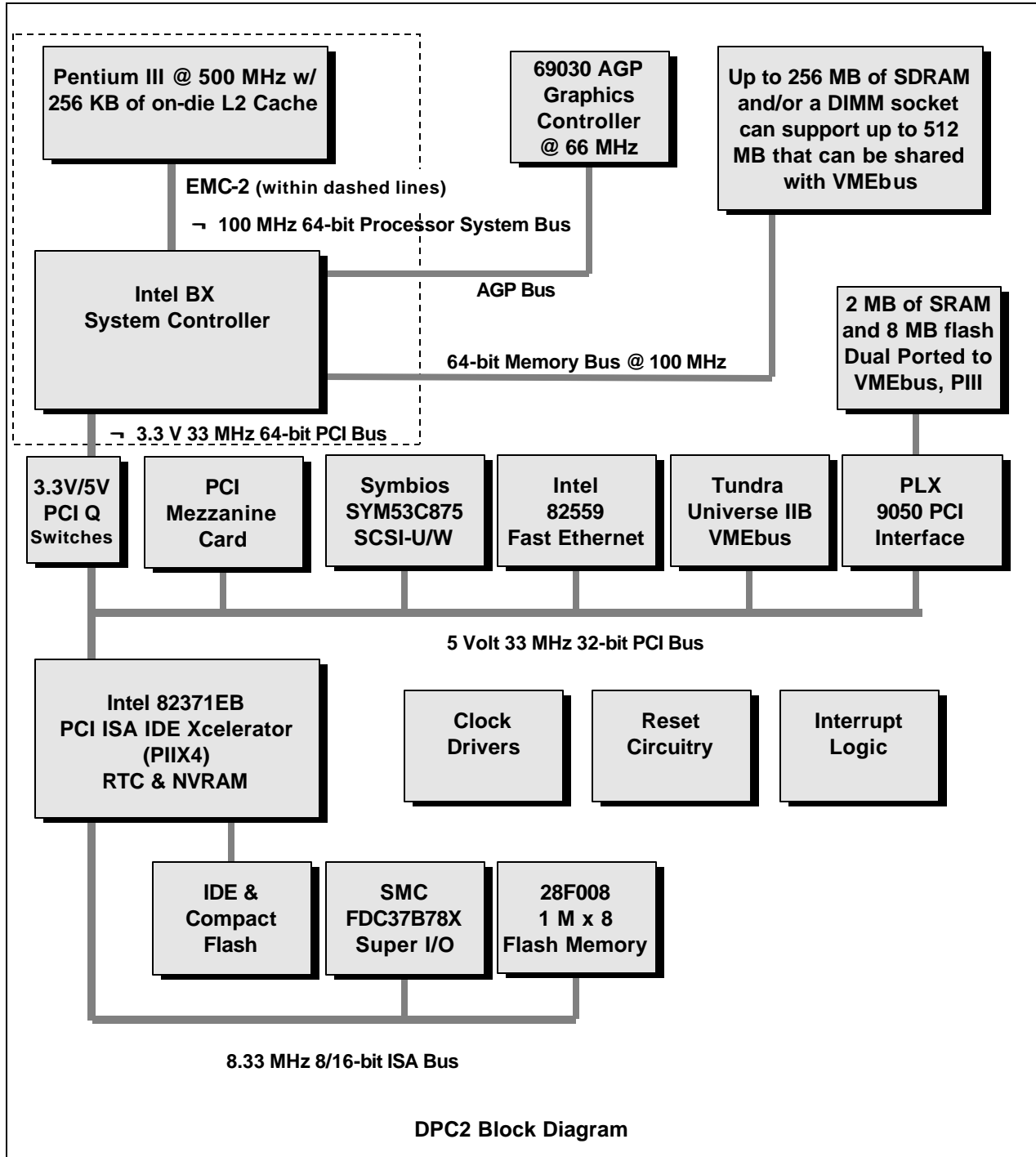
The following documents are the current draft standards for the PCI Mezzanine Card (PMC):

- IEEE Draft Std P1386/2.0, *Draft Standard for a Common Mezzanine Card Family: CMC*  
The Institute of Electrical and Electronic Engineers  
345 East 47th Street  
New York, NY 10017  
(800) 678-4333
- IEEE Draft Std P1386.1/2.0, *Draft Standard Physical and Environmental Layers for PCI Mezzanine Cards: PMC*  
The Institute of Electrical and Electronic Engineers  
345 East 47th Street  
New York, NY 10017  
(800) 678-4333

### 3. Hardware Description

#### 3.1 Overview

The block diagram of the DPC2 is shown below. The sections that follow describe the major functional blocks of the DPC2.



### 3.2 Pentium III Processor

The DPC2 supports a low-power mobile Pentium III processor with a clock speed of 500 MHz. This Pentium III processor's features include:

- 100 MHz Processor System Bus (PSB).
- Built-in Level 1 instruction (code) and data caches of 16 KB each and 256 KB of on-die L2 cache.
- Integrated math co-processor.
- Power management, MMX, and backwards compatibility with Pentium class processors.

For further information on the Pentium processor, refer to *Pentium Processors and Related Products*, available from Intel Corporation.

### 3.3 Intel 82443BX Chipset

The Intel BX chipset consists of two devices: the 82443BX System Controller (BX), also known as the “Northbridge”, and the FW82371EB PCI ISA IDE Xcelerator (PIIX4E), a.k.a. the “Southbridge”. The BX integrates the following functions into a single ball-grid array (BGA) package:

- 66 MHz AGP Interface.
- 100 MHz DRAM controller supporting two 64 MB banks of Synchronous DRAM (SDRAM) each with a 64-bit interface and two additional banks which are routed to a 168-pin DIMM connector.
- PCI 2.1 compliant, high-performance Processor-to-PCI buffered bridge with PCI bus arbitration logic.

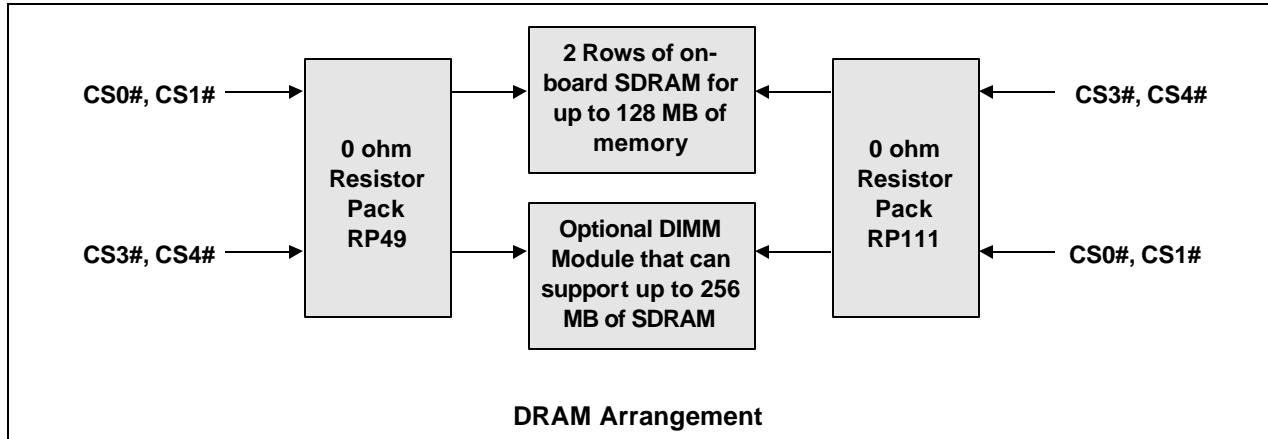
The PIIX4 integrates the following functions into a single ball-grid array (BGA) package:

- PCI-ISA bridge with PCI interrupt steering logic for Plug-n-Play support.
- Primary and secondary Ultra DMA/33 PCI IDE interfaces. The IDE signals are brought out to J7 and J10. The primary IDE port, J7, is a 44-pin dual-row 2-mm header on the PCB. The secondary port, J10, is a CompactFlash Type II connector. The pin-outs for these connectors are given in Appendix A.
- Standard PC 82C54 timer, 82C59 programmable interrupt controller (PIC), Real Time Clock, NVRAM, and 82C37 DMA controller functions.

For further information, see the documents referenced in Section 2.

### 3.4 DRAM

The DPC2 offers up to 128 MB of Synchronous DRAM (SDRAM) on-board and also features a 168-pin DIMM socket for additional 3.3 V PC100 SDRAM memory. The maximum amount of DRAM that the BX Northbridge device can address with its four select lines would be 384 MB. Versions of the DPC2 with 384 MB of DRAM divide the range so that 128 MB would be on-board and the remaining 256 MB would be on the DIMM socket. The DPC2 will be configured at the factory for on-board DRAM (2 rows selected) & DIMM (with only 2 out of 4 bank selects routed) or only DIMM (for a maximum DRAM capacity of 256 MB). When the DPC2 is shipped with on-board SDRAM, this memory will be mapped at the base location (Resistor pack RP49 is populated). When the DPC2 is shipped without on-board SDRAM, the DIMM module will be mapped to the bottom of the memory map (RP111 is populated).



The DRAM controller is described in more detail in *Intel 82443BX AGPset – 82443BX Host/Bridge Controller Datasheet*, available from Intel Corporation.

### 3.5 Asilient 69030 HiQVideo™ Accelerator with 4 MB SDRAM

The 69030 HiQVideo Accelerator offers the following features:

- 4 MB of embedded SDRAM with a 100 MHz operation for up to 800 MB/s frame buffer bandwidth.
- 66 MHz AGP interface with the 82443BX Northbridge Chip, independent of the PCI bus.
- Supports resolutions up to 1600 x 1200 x 64 K @ 60 Hz and True Color 24 bits per pixel in lower resolutions.

The analog CRT signals are brought out to J2, a DB15F connector on the front panel.

For further information on the 69030, refer to *Asilient 69030 HiQVideo™ Accelerator with 4-MB SDRAM Databook Rev. 1.3*, which can be downloaded from [http://www.asilient.com/pdf/ds182\\_3.pdf](http://www.asilient.com/pdf/ds182_3.pdf)

### 3.6 Symbios SYM53C875 Ultra Wide SCSI Controller

The Symbios SYM53C875 offers the following features:

- Ultra wide SCSI synchronous transfers up to 40 MB/sec, asynchronous rates up to 20 MB/sec.
- Includes 4 KB of internal RAM for SCRIPTS instruction storage.
- Full 32-bit PCI DMA master.
- Performs zero wait-state bus master data bursts faster than 110 MB/sec.

The 16-bit SCSI bus data and control signals are terminated on the DPC2 via Dallas Semiconductor DS21S07AE active terminators (turned on when jumper JP17 is open), and terminating power is supplied to the SCSI bus via a 1 amp self-resetting fuse (F5). The SCSI bus signals are brought out to user-defined pins on the VMEbus P2 connector. The pin-out for P2 is given in Appendix A.

## Chapter 3 – Hardware Description

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The SYM53C875 contains several PCI configuration registers. It also contains a number of device registers that can be mapped to the memory space or the I/O space. The PCI signals specific to the Symbios SYM53C875 are shown below:

Symbios SYM53C875 Signal	PCI Bus Connection
IDSEL	AD24 (PCI Device 0Dh)
PREQ#	REQ2# (82443BX)
GNT#	GNT2# (82443BX)
IRQA#	PIRQA# (PIIX4)

For further information on the SYM53C875, refer to *SYM53C875 PCI-Ultra SCSI I/O Processor Data Manual Version 3.0*. Symbios' SCSI products were taken over by LSI Logic. For downloadable data, please go to [http://www.lsilogic.com/products/storage\\_standard\\_prod/oem/iocontrollers/products/ultracontrollers.html#875E](http://www.lsilogic.com/products/storage_standard_prod/oem/iocontrollers/products/ultracontrollers.html#875E)

### 3.7 Intel 82559 Fast Ethernet Controller

The Intel 82559 offers the following features:

- 10BaseT and 100BaseTX support with auto-negotiation.
- Independent 3 KB receive and transmit FIFOs.
- Powerful on-chip DMA minimizes CPU overhead with zero wait-state burst transfers to system memory.
- Built-in Phyceiver.
- Serial EEPROM for nonvolatile Ethernet address storage.

The 10BaseT/100BaseTX signals are brought out to J4, an RJ-45 connector on the front panel. The pin-out for J4 is given in Appendix A. Three front panel LEDs are located between the VGA connector and the Keyboard/Mouse connector and are controlled by the Ethernet circuitry: CR1 is next to the VGA port (it is on when transferring at 100 Mb/sec, off when transferring at 10 Mb/sec), CR2 is in the middle (active), and CR3 is next to the keyboard/mouse port (link established).

The Intel 82559 contains several PCI configuration registers. It also contains a number of device registers for controlling the Ethernet operation that can be mapped to the memory space or the I/O space. The PCI signals specific to the Intel 82559 are shown below:

Intel 82559 Signal	PCI Bus Connection
IDSEL	AD23 (PCI Device 0Ch)
PREQ	REQ0# (82443BX)
PGNT	GNT0# (82443BX)
PIRQ	PIRQC# (PIIX4)

For further information on the 82559, refer to *82559 Fast Ethernet Multifunction PCI/Cardbus Controller*, available from Intel Corporation. Please go to the link at: <http://developer.intel.com/design/network/products/lan/controllers/82559.htm>

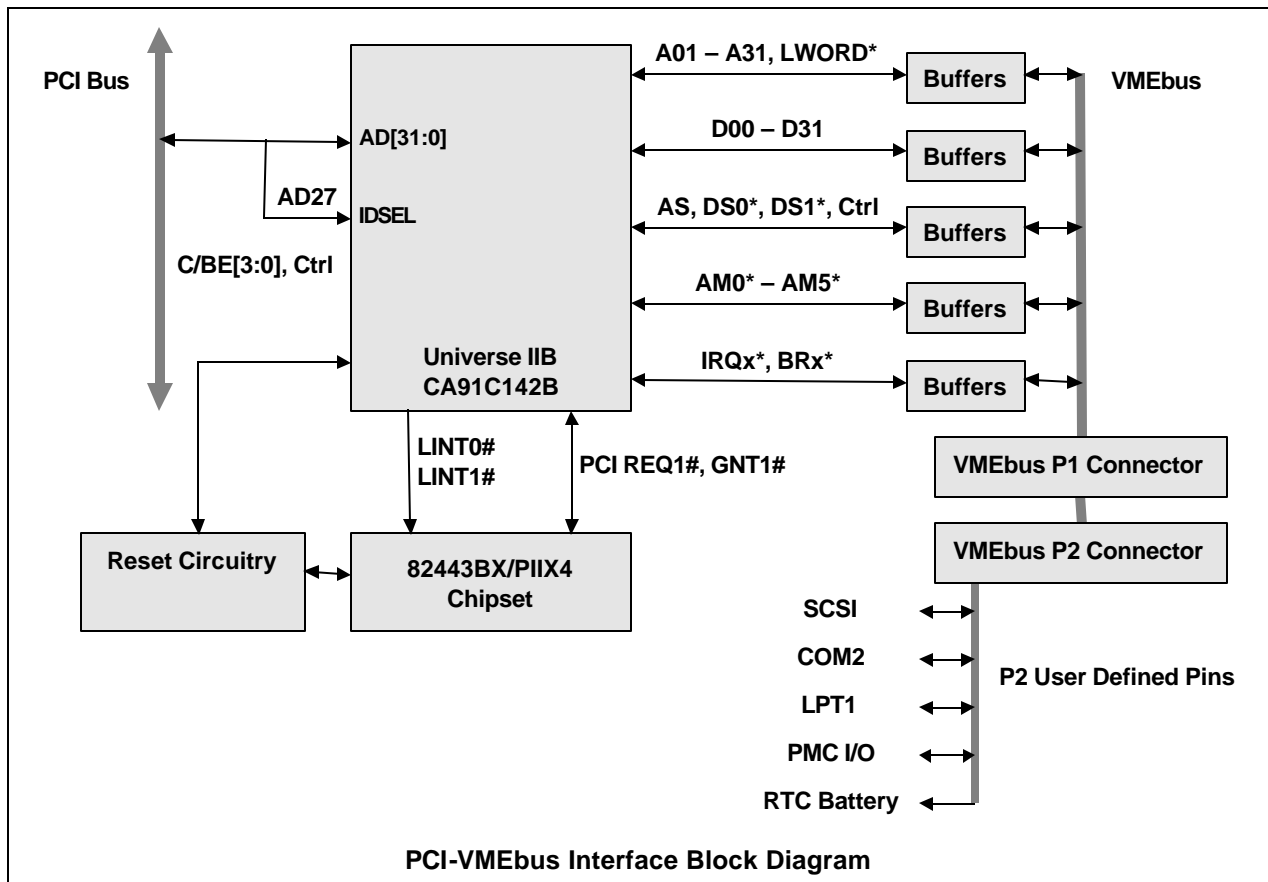
### 3.8 Tundra Universe IIB CA91C142B PCI-VMEbus Interface

The PCI-VMEbus interface, based on the Tundra Universe IIB CA91C142B, offers the following features:

- High-performance 64-bit VMEbus interface.
- Integral FIFOs for write-posting allow the Universe IIB to quickly relinquish the bus.
- Programmable DMA controller with linked list support.
- Full VMEbus system controller functionality.
- Complete VMEbus address and data transfer modes:
  - A32/A24/A16 master and slave
  - D64 (MBLT)/D32/D16/D08 master and slave
- Flexible register set, programmable from both the PCI bus and the VMEbus.

There is a caveat associated with using the Universe IIB for sharing system DRAM with the VMEbus while simultaneously performing write operations to the VMEbus that is addressed in Section 3.10.2.

The block diagram of the PCI-VMEbus interface is shown below:



## Chapter 3 – Hardware Description

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As shown in the block diagram, several peripheral signals are routed to the user-defined pins of the VMEbus P2 connector. The VMEbus P1 and P2 connector pin-outs are given in Appendix A.

The Universe IIB CA91C142B can act as a PCI bus initiator (master) or target (slave), and a VMEbus master or slave. The Universe IIB is capable of generating interrupts on the VMEbus, and can act as a VMEbus interrupt handler. Full VMEbus system controller functionality is provided by the Universe IIB. The DPC2 reset circuitry is tied to the Universe IIB, since the DPC2 can generate the VMEbus SYSRESET\* signal as well as be reset by another VMEbus board that asserts the SYSRESET\* signal. The DPC2 reset circuitry is discussed in detail in Section 3.16.

This section is intended to supplement the Universe IIB section of the *VMEbus Interface Components Manual*, which contains comprehensive descriptions of the operation and programming of the Universe IIB. In that manual, Chapter 2, *Functional Description*, Appendix A, *Registers*, and Appendix E, *Cycle Mapping*, provide the necessary information to understand the operating modes of the Universe IIB:

- DPC2-initiated transfers (PCI slave, VMEbus master).
- Other VMEbus master-initiated transfers (PCI master, VMEbus slave).
- DMA controller transfers (PCI master, VMEbus master).
- VMEbus interrupt generation.
- VMEbus interrupt handling.
- System controller functionality.
- Register programming via the PCI bus and the VMEbus.
- Coupled and uncoupled transfers between the PCI bus and the VMEbus.
- 4 mailboxes and 8 semaphores.
- VMEbus arbitration.

The Universe IIB Control and Status Registers (UCSRs) are used for the configuration of the Universe IIB. These registers form a 4 KB block, divided into three groups:

- PCI Configuration Space (PCICS).
- Universe IIB Device Specific Status Registers (UDSRs).
- VMEbus Control and Status Registers (VCSRs).

These registers are accessible (to varying degrees) via three address spaces:

- PCI Configuration Space – Only the PCICS register block is accessible in this space.
- PCI Memory Space – The entire 4 KB UCSR block is accessible in this space.
- VMEbus A32/A24/A16 Space – The entire 4 KB UCSR block is accessible in this space.

During initialization, the system BIOS maps PCI peripherals that require space beyond the PCI configuration space into the memory space or I/O space. The Universe IIB UCSR block is 4 KB in size and must be aligned on a 64 KB boundary. The total I/O space of an Intel processor is 64 KB and many of the common PC peripherals are found in the first 1 KB of this space. Thus, a request for a 64 KB block of I/O space for the Universe IIB registers would be denied by the system BIOS, leaving the Universe IIB unmapped. To avoid this situation, the Universe IIB offers a power-up option to map its registers into the memory space. This is accomplished on the DPC2 by tying the VA[1] line high via a pull-up resistor.

There are two mechanisms to access the UCSR block from the VMEbus. The first is the VMEbus Register Access Image (VRAI) method, which is defined by the following registers in the Universe IIB section of the *VMEbus Interface Components Manual*:

Field	Register Bits	Description
Address Space	VAS in Table A.76	A32, A24, or A16
Base Address	BS[31:12] in Table A.77	Lowest address in the 4 KB slave image
Slave Image Enable	EN in Table A.76	Enable VMEbus Register Access Image
Mode	SUPER in Table A.76	Supervisor and/or Non-Privileged
Type	PGM in Table A.76	Program and/or Data

The reset state of the VAS, BS[31:12], and EN fields can be configured as power-up options. On the DPC2, all of these fields reset to 0. Thus, the VRAI method must be configured and enabled by accessing the Universe IIB registers in the memory space.

The second mechanism for accessing the UCSR block from the VMEbus is the CS/CSR method, which is defined by the following registers in the Universe IIB section of the *VMEbus Interface Components Manual*:

Field	Register Bits	Description
Base Address	BS[23:19] in Table A.84	Base address of Universe IIB 512 KB slot
Slave Image Enable	EN in Table A.78	Enable CS/CSR image

The BS[23:19] and EN fields reset to all 0s, and the EN bit can be set by the VME64 Auto ID process. Thus, the CR/CSR method must be configured by accessing the Universe IIB registers in the memory space.

The PCI signals specific to the Tundra Universe IIB CA91C142B are shown below:

Tundra Universe IIB CA91C142B Signal	PCI Bus Connection
IDSEL	AD27 (PCI Device 10h)
REQ#	REQ1# (82443BX)
GNT#	GNT1# (82443BX)
LINT0#	PIRQB# (PIIX4)
LINT1#	EXTSMI# (PIIX4)

### 3.9 PCI Mezzanine Card (PMC) Slot

The PMC Slot offers the following characteristics:

- Conforms to IEEE draft standards 1386/2.0 and 1386.1/2.0.
- Accepts single-width 5V PMC boards with front panel I/O.
- Provides 32-bit PCI support via connectors JN1 and JN2, and JN4 is available for routing PMC I/O to VMEbus connector P2. The DPC2 does not contain a JN3 connector for 64-bit PCI support, but cards containing a PN3 connector are accommodated (that is, no components on the DPC2 interfere with a PMC PN3 connector).

The PCI signals specific to the PMC Slot are shown below:

PMC Slot Signal	PCI Bus Connection
IDSEL	AD26 (PCI Device 0Fh)
REQ#	REQ3# (BX)
GNT#	GNT3# (BX)
PMCINTA#	PIRQD# (PIIX4)
PMCINTB#	JP19
PMCINTC#	JP20, JP18
PMCINTD#	PIRQD# (PIIX4)

On earlier VMEbus PC's, Dynatem tied all of the PMCINT lines together as we were using only one PMC support site (a single PMC card should not require more than one interrupt). Since the XPMC3 can now expand this one slot to three additional sites in a second VMEbus slot, we have broken out the first three PMCINT lines as you can see above (PMCINTA# and PMCINTD# are both brought to the available PIRQD# of the PIIX4 Southbridge (and PIRQD# is internally channeled to IRQ5 in the PIIX4)). The customer has the option of routing PMCINTB# and PMCINTC# to unused lines (IRQ7 which is normally used by LPT1) or sharing them with the DPC2's PCI options that may be left off or not used like the Universe IIB or the 53C875 SCSI controller. The following table shows how PMCINTB# and PMCINTC# may be routed to the PIIX4 as configured by jumpers JP18, JP19, and JP20 (Pin 1 of each jumper is designated by a square pad on the DPC2 PCB):

PMC Interrupt Routing to the PIIX4	Jumper Settings
PMCINTB# is routed to IRQ7	JP19 is shunted between pins 1 & 2
PMCINTB# is routed to PIRQA# (Usually used by the SCSI port)	JP19 is shunted between pins 2 & 3
PMCINTC# is routed to IRQ7	JP20 is shunted between pins 1 & 2
PMCINTC# is routed to PIRQD#	JP20 is shunted between pins 2 & 3
PMCINTC# is routed to PIRQB# (Usually used by the Universe IIB)	JP18 is shunted

PIRQD# is internally routed to IRQ5 in the PIIX4.

The XPMC3 routes the PMCINT lines directly from the host adapter connectors to the expansion slot connectors. In other words, PMCINTA# on any expansion slot on the XPMC3 will route directly to PMCINTA# on the DPC2's PMC site when the XPMC3 is installed on the DPC2.

For further information on the PMC specification, refer to *PCI Local Bus Specification, Revision 2.1*, available from the PCI Special Interest Group, IEEE Draft Std P1386/2.0, *Draft Standard for a Common Mezzanine Card Family: CMC*, and IEEE Draft Std P1386.1/2.0, *Draft Standard Physical and Environmental Layers for PCI Mezzanine Cards: PMC*, both available from the Institute of Electrical and Electronic Engineers.

### 3.10 PLX PCI9050-1 PCI Interface For Dual Port Memory

With the DPC2, Dynattem decided to offer both expanded on-board flash memory, beyond what could be supported in the 1 MB of “real mode” address space, and 2 MB of additional battery-backed SRAM. The PLX PCI9050-1 is a PCI peripheral adapter that lets the local processor access this memory as well as alternate masters on the VMEbus. The PCI9050-1 cannot be a PCI master device and therefore does not have REQ# or GNT# signals. Neither does it generate interrupts as implemented on the DPC2. Since it is simply a memory interface, none of these capabilities are needed. The PCI signals for the PCI9050-1 are defined below:

PMC Slot Signal	PCI Bus Connection
IDSEL	AD22 (PCI Device 0Bh)
REQ#	Not Applicable
GNT#	Not Applicable
INT#	Not Applicable

The DPC2 can support an 8 MB flash ROM on the DPC2 that can be mapped into PCI memory. This device can hold BIOS extensions, a compact OS, and application code and let the user boot up free of a mechanical boot device or even a CompactFlash device. This is PCI accessible memory.

The DPC2 also optionally provides 2 MB of SRAM. This on-board SRAM is battery-backed by the same circuit that backs up the RTC and the BIOS’s NV-RAM in the PIIX4 Southbridge chip. These non-volatile devices draw their power-down current from the on-board lithium coin cell labeled BT1. They can also draw power from one of two pins on the VMEbus backplane: standard auxiliary power line +5VSTDBY on P1 pin B31 or a proprietary pin labeled by Dynattem as RTCBAT on P2 pin C13.

2 MB is a limited amount of memory but it serves two purposes that make it convenient shared memory between the VMEbus and the local Pentium III processor.

#### 3.10.1 Big/Little Endian Translation

While the Pentium III accesses memory by little endian addressing, many other processor families that are commonly found on VMEbus modules (e.g., Motorola’s 68K MPUs and PowerPC processors) use big endian addressing. Little endian processors access the least significant bytes in multi-byte words first. This is a common conflict when using x86 (Intel CPUs including the Pentium III) processors on the VMEbus. The solution is generally to do software byte swapping to observe consistent data integrity. The negative with this approach is the software overhead required. The shared SRAM behind the PCI9050-1 solves this problem by using big endian addressing when the memory is accessed from the VMEbus and little endian addressing when the local Pentium III accesses the memory. Therefore, no byte juggling is required and the memory space can easily be shared.

Note: The SRAM can also be accessed from the VMEbus in the little endian mode (if the VMEbus master uses another x86 processor for instance) by addressing the SRAM at the same PCI address range that the Pentium III uses locally.

### 3.10.2 Preventing PCI/VMEbus Contention

The second issue is more complicated. There is a specific situation where the DPC2 can enter a deadly embrace scenario and hang up. This can potentially happen when system DRAM is shared with the VMEbus and the DPC2 is performing a coupled write data transfer to the VMEbus. When the Northbridge chip, the 82443BX, is performing a write operation, the passage to system DRAM is blocked from access by any PCI devices other than the Universe III. In other words, no other PCI device (which includes another VMEbus master via the DPC2's Universe IIB) can read from or write to the DPC2's system DRAM while the DPC2's 82443BX is performing a write cycle to the VMEbus. So during a coupled write to the VMEbus ("coupled" specifies that it will not be completed locally until it is completed on the VMEbus), another VMEbus master will not be able to access the system DRAM and a deadly embrace ensues: the DPC2 cannot conclude its coupled write to the VMEbus as another VMEbus master has possession of the VMEbus and this master cannot terminate its cycle as it cannot access the DPC2's system DRAM. The Universe IIB will do continuous PCI retry operations to no avail, as the 82443BX will never terminate its coupled write to the VMEbus. If the VMEbus specification mandated retry cycles or if the 82443BX supported DRAM accesses during a write cycle, there would be no problem.

If the user needs to share memory with the VMEbus and perform data write transfers to the VMEbus, possibly concurrently, there are two ways around this problem. The first is to only perform posted write cycles to the VMEbus through the Universe IIB. Coupled write cycles lock the PCI bus with the VMEbus and the transfer on the PCI bus is not completed until it is completed on the VMEbus. Posted write cycles use the TxFIFO in the Universe IIB. The Pentium III will write to the TxFIFO and then the Universe IIB will independently write to the VMEbus. The posted write mode will empty the 82443BX chip's FIFO so that DRAM will be accessible from the VMEbus. The negative with this solution is that when the Universe IIB's TxFIFO fills up and overflows, the write cycles will then become coupled. Therefore the TxFIFO needs to be monitored. The TxFIFO holds thirty-two 64-bit wide entries. Please consult the Universe IIB User's Manual from Tundra for more information on handling the TxFIFO. There is a status bit in the Universe IIB's MISC\_STAT register called "TXFE" which is high when the TxFIFO is empty. So, under software control, the user should ensure that the TxFIFO is first empty before loading it and then take precautions not to continue loading it after it has been filled. This obviously will require some software overhead.

The second approach to this problem would be to use the 2 MB of on-board SRAM that can be accessed by the local Pentium III and other VMEbus masters with no issues regarding bus contention. 2 MB of SRAM may not seem like a lot of memory but it can be used for holding small data buffers or for messaging in multi-processing applications.

**3.11 SMSC FDC37B78x Multi I/O Controller**

The SMSC FDC37B78x provides the following standard PC peripherals:

- Floppy drive controller with support for drives up to 2.88 MB.
- COM1 and COM2 serial ports, based on 16C550 compatible UARTs with 16-byte transmit and receive FIFOs.
- LPT1 parallel port that’s capable of standard, bidirectional, enhanced parallel port (EPP), and enhanced capabilities port (ECP) operation, with IEEE 1284 compliance.

The FDC37B78x CLK1 input is driven by a 24 MHz clock, with CLK2 left unconnected.

The floppy drive signals are routed to J11, a 1.00mm ZIF flex circuit connector on the PCB. The COM1 signals are brought out to J3, a DB9M connector on the front panel. The COM2 and LPT1 signals are routed to the user defined pins of the VMEbus P2 connector. The connector pin-outs are given in Appendix A.

The SMSC FDC37B78x I/O space addresses upon power-up or reset are shown below:

SMSC FDC37B78x Register	I/O Address
Configuration	3F0, 3F1
COM1	3F8 - 3FF
COM2	2F8 - 2FF
Parallel Port	278 - 27F
Floppy Drive Interface	3F0 - 3F7

The FDC37B78x defaults to LPT2 (278-27F) upon power-up or reset, but the system BIOS can reconfigure the parallel port for operation as LPT1 (378-37F), LPT2 (278-27F), or LPT3 (3BC-3BF). Thus, throughout this manual the parallel port is referred to as LPT1.

The SMSC FDC37B78x interrupt request line assignments are shown below:

SMSC FDC37B78x Function	Interrupt Request Line
COM2, COM4	IRQ3
COM1, COM3	IRQ4
LPT2	IRQ5
Floppy	IRQ6
LPT1	IRQ7

The SMSC FDC37B78x DMA channel assignments are shown below:

SMSC FDC37B78x Function	DMA Channel
Floppy	DMA Channel 2
Parallel Port (ECP mode)	DMA Channel 5

## Chapter 3 – Hardware Description

The keyboard/mouse controller, based on the Intel 8042, is built-in to the FDC37B78x and it is a standard 8-bit ISA peripheral for controlling a PS/2 style keyboard and a PS/2 style mouse. Power is supplied to the keyboard and mouse via a 1 amp self-resetting fuse (F1). The keyboard and mouse signals are routed to J1, which is a 6-pin mini-DIN receptacle on the front panel. The pin-out of J1 is given in Appendix A.

The FDC37B78's keyboard/mouse controller I/O space addresses are shown below:

FDC37B78's Keyboard/Mouse Controller Register	I/O Address
Keyboard/Mouse Data	60
Keyboard/Mouse Status/Command	64

The FDC37B78's keyboard/mouse controller interrupt request line assignments are shown below:

FDC37B78's Keyboard/Mouse Controller Function	Interrupt Request Line
Keyboard Buffer Full	IRQ1
Mouse Buffer Full	IRQ12

For further information on the FDC37B78x, refer to the *FDC37B78x Data Sheet*, available from Standard Microsystems Corporation, their website is at <http://www.smsc.com/>

### 3.12 Real Time Clock and NVRAM

Both the Real Time Clock (RTC) and the NVRAM for holding battery-backed BIOS parameters are contained within the 82371AB PCI ISA IDE Xcelerator (PIIX4). The RTC generates IRQ8. NVRAM addresses use I/O address 70 while NVRAM data use I/O address 71. Please refer to the third paragraph in Section 3.10 for more information on how the PIIX4 is battery-backed.

### 3.13 Intel 28F008B3 System BIOS Flash Memory

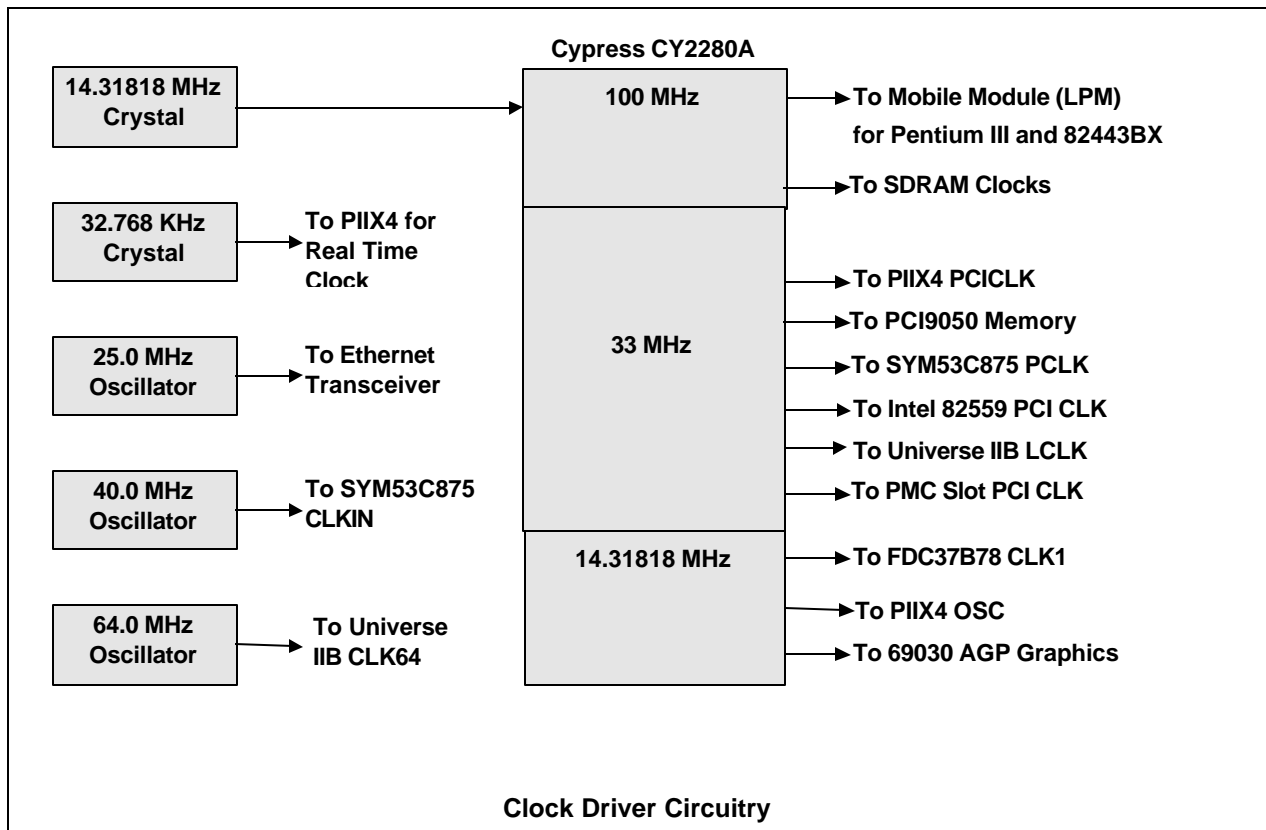
The Intel 28F008B3 is a 120-nsec, 1 Mb x 8 flash memory for the system BIOS. This device can fill the 1 MB real mode memory map so only a portion, the upper 256 MB, of it is used. The 28F008B3's 1 MB of memory space is segmented into eight parameter blocks of 8 KB each at the top of memory, and fifteen main blocks of 64 KB each below that. The DPC2 powers up into real mode and the BIOS is eventually shadowed into system DRAM after booting through the BIOS. Here is how the 82443BX Northbridge chip maps the real mode:

Real Mode Address Range	Block Description
00000 - 7FFFF (512 KB)	DOS Area RAM
80000 - 9FFFF (128 KB)	Optional Fixed Memory Hole
A0000 - BFFFF (128 KB)	BIOS Startup Video RAM
C0000 - DFFFF (128 KB)	28F008's BIOS for Video Controller
E0000 - FFFFF (128 KB)	28F008's General System BIOS

The 82371AB (PIIX4) provides the chip select signal to the 28F008B3, which is an 8-bit ISA device. The upper 256 KB of the 28F008B3 is located from 000C0000 - 000FFFFFF (the top of 1 MB) and its full 1 MB of memory is aliased from FFF00000 – FFFFFFFF where it can be fully accessed after booting up through the BIOS.

### 3.14 Clock Drivers

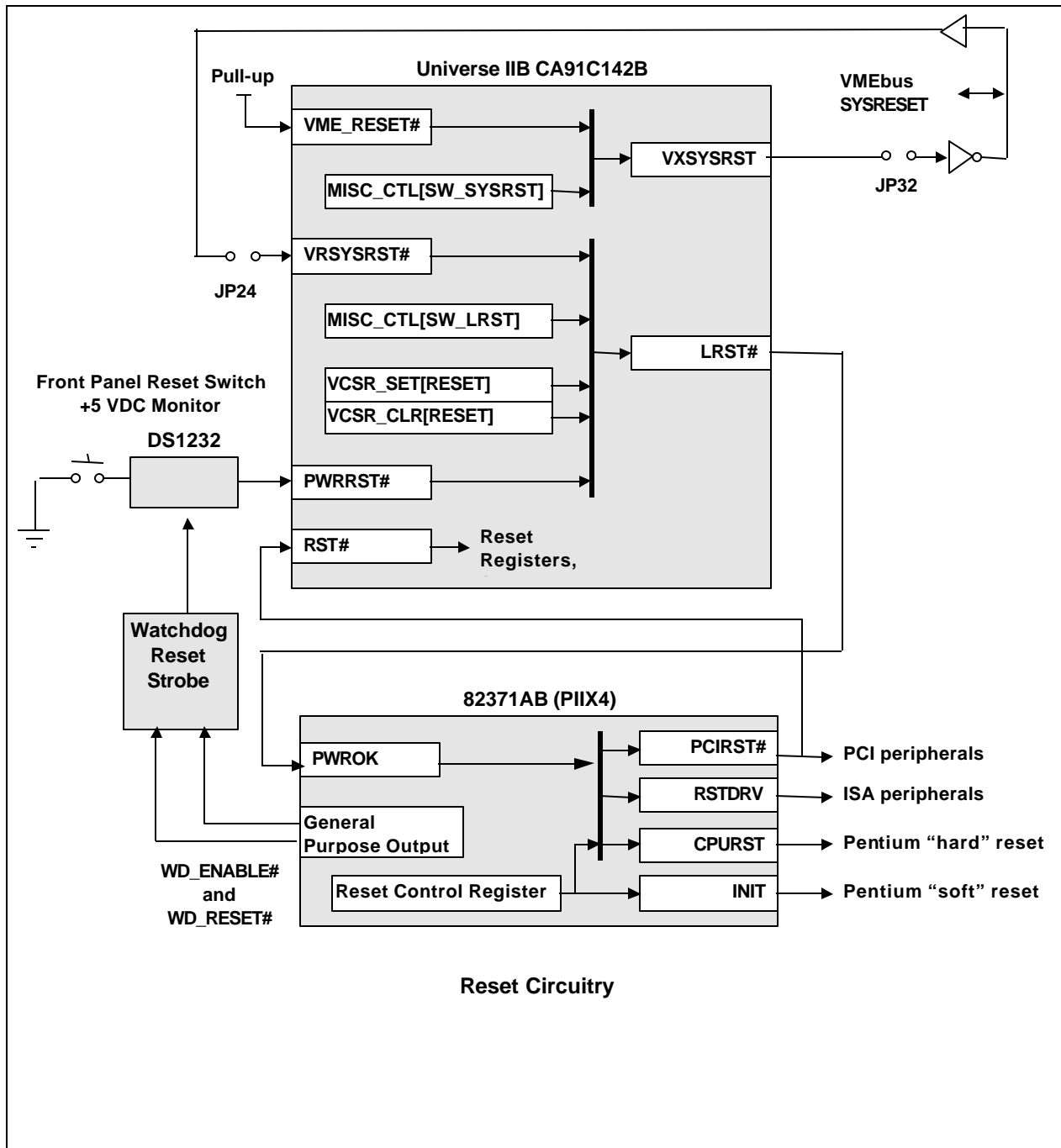
The clock driver circuitry is shown below:



The clock driver circuitry is based on the Cypress CY2280A, driven by a 14.31818 MHz crystal. A 32.768 KHz Crystal drives the Real Time Clock (RTC) to the PIIX4, a 25.0 MHz oscillator drives the Ethernet transceiver circuitry, a 40.0 MHz oscillator drives the SYM53C875 SCSI bus circuitry, and a 64.0 MHz oscillator drives the Universe IIB CA91C142B VMEbus circuitry.

## 3.15 Reset Circuitry

The reset circuitry is shown below:



When the Universe IIB is not used (as on the XPC2), the PWRRST# to LRST# chain is bypassed by shunting JP21.

Opening JP28 will prevent the DPC2's hard reset from resetting the VMEbus backplane (see next page).

Opening JP23 will isolate the DPC2 from VMEbus SYSRESETs.

There are eight ways to perform a hard reset of the DPC2:

- The DS1232 senses that the +5 VDC supply has dropped too low, which asserts the Universe IIB PWRRST# input.
- The front panel reset switch is pressed, which asserts the Universe IIB PWRRST# input.
- Another VMEbus board asserts SYSRESET\*, which asserts the Universe IIB VRSYSRST# input (unless JP23 is open).
- The SW\_SYSRST bit in the MISC\_CTL register of the Universe IIB is set by code running on the DPC2 processor. This leads to the assertion of the VMEbus SYSRESET\* signal as well as a local reset of the DPC2 board circuitry.
- The SW\_LRST bit in the MISC\_CTL register of the Universe IIB is set by code running on the DPC2 processor. This performs a local hard reset of the DPC2 board circuitry without asserting the VMEbus SYSRESET\* signal.
- Another VMEbus master sets the RESET bit in the VCSR\_SET register of the Universe IIB over the VMEbus. In this case the LRST# signals remains asserted until the RESET bit of the VCSR\_CLR register of the Universe IIB is set by another VMEbus master over the VMEbus.
- The Reset Control register in the PIIX4 can be set appropriately by code running on the DPC2 processor.
- Let the watchdog timer time out; see Section 3.16 below.

There are two ways to assert the Pentium processor INIT signal, leading to a local soft reset of the DPC2 without asserting the VMEbus SYSRESET\* signal:

- The FDC37B78's keyboard/mouse controller P20 output can be brought low via code running on the DPC2 processor.
- The Reset Control register in the PIIX4 can be set appropriately by code running on the DPC2 processor.

For further information on the peripherals that play a part in the reset circuitry, refer to *Intel 430BX AGPset – 82443BX Host Bridge/Controller Datasheet* from Intel Corporation, Document Number 290633-001, and *Intel 82371AB (PIIX4) PCI ISA IDE Xcelerator Specification Update*, also available from Intel Corporation at [www.intel.com](http://www.intel.com), *Universe II User Manual* and the *Universe IIB(CA91C142B) Device Errata*, available from Tundra Semiconductor Corporation at [www.tundra.com](http://www.tundra.com), and the *FDC37B78x Data Sheet*, available from Standard Microsystems Corporation. Their website is at [www.smsc.com](http://www.smsc.com).

### 3.16 Watchdog Timer Operation

The DPC2 features a watchdog timer, which can be implemented as a safeguard against the system hanging up. The PLD controlling the Dallas DS1232 has two inputs, which are called WD\_ENABLE# and WD\_RESET#.

WD\_ENABLE# is the GPO0 output of the PIIX4 and WD\_RESET# is the GPO8 output of the PIIX4. While WD\_ENABLE# is high, the PLD pulses the ST# input to the DS1232 constantly so it will not generate a reset unless the power drops or the front panel push button is pressed. When WD\_ENABLE# is brought low, the WD\_RESET# line must be toggled low, then high, to produce a ST# pulse to the DS1232. If the ST# input to the DS1232 is not produced within the watchdog timer timeout period (which is a minimum of 1.2 seconds), the DS1232 resets the board as if the front panel reset button had been pushed.

## Chapter 3 – Hardware Description

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**Both GPO0 and GPO8 reset to high** so the watchdog is disabled by a reset. It is only after WD\_ENABLE# (GPO0) is driven low that the watchdog timer is in danger of timing out and resetting the board.

Both WD\_ENABLE# and WD\_RESET# are controlled via the PIIX4 PCI Function 3 (Power Management) GPOREG register. The GPOREG register is mapped into I/O space at PCI configuration time, at an offset of 34h from the Function 3 I/O base address set in the PMBA (Power Management Base Address) register at offset 40h in the Function 3 PCI configuration space.

Each PCI function (whether in a single-function or multi-function device) with control registers has one or more base address register in its configuration space. The PCI configuration process goes through each function, determines its register mapping requirements, and maps its registers to I/O or memory space. The control registers of the PIIX4 PCI Function 3 are always mapped to I/O space, and their base address is stored at offset 40h within the PCI configuration space for that function. The GPOREG is at offset 34h from that base address.

To write a device driver for the watchdog timer, there are standard means from within the driver to determine the base address for the registers of a given PCI function. The device driver would then have functions to enable, disable, and reset the watchdog timer.

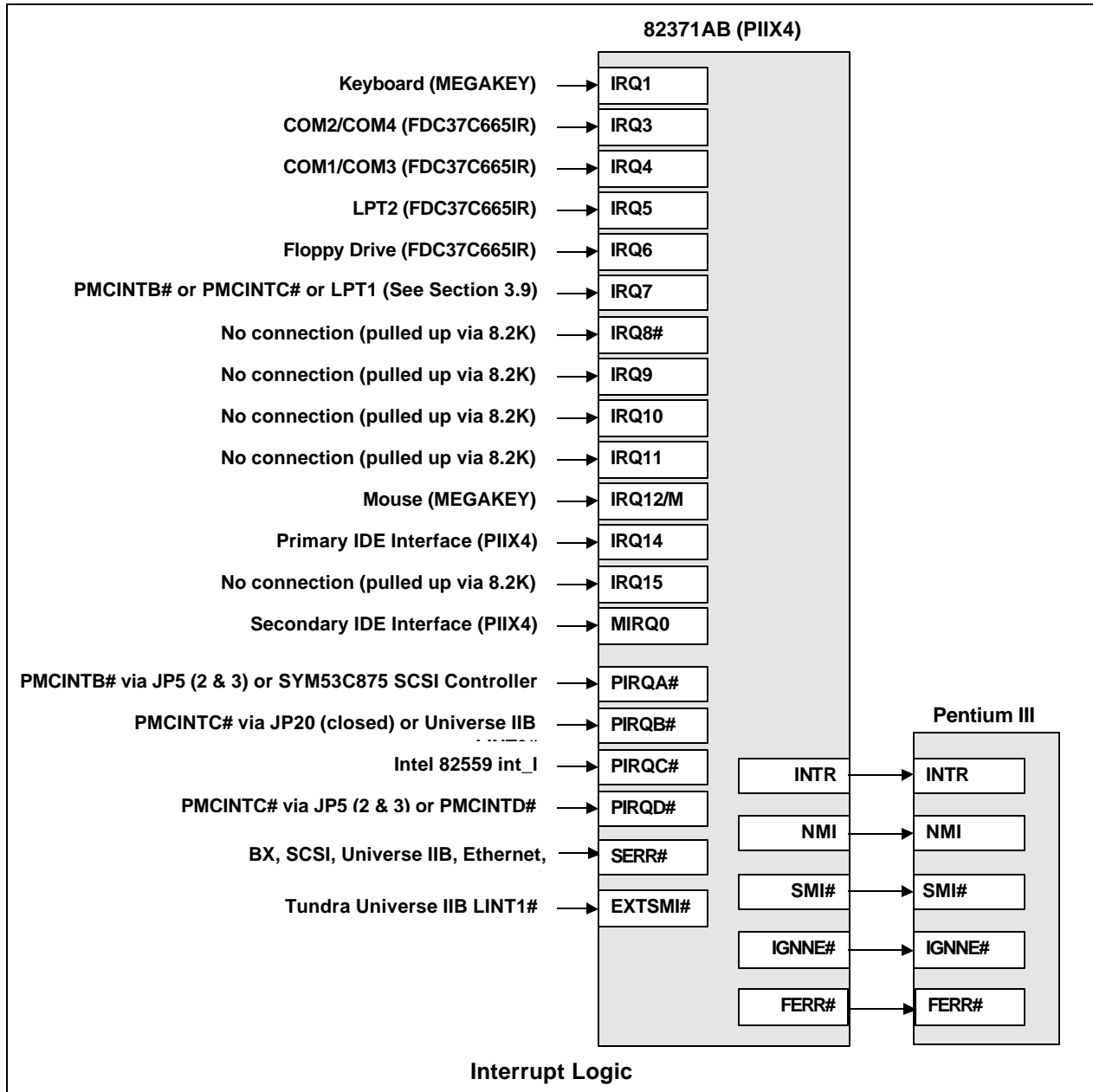
To enable the watchdog timer, bit 0 of GPOREG is set to 0.

To disable the watchdog timer, bit 0 of GPOREG is set to 1.

To reset the watchdog timer, bit 8 of GPOREG is set to 0 then 1.

3.17 Interrupt Logic

The interrupt logic is shown below:



The DPC2 follows the standard PC ISA interrupt assignments. Logic in the PIIX4 can steer the four PCI interrupts to selected ISA interrupts.

The Universe IIB CA91C142B is capable of acting as an interrupter and interrupt handler for the VMEbus, and can generate PCI interrupts in response to VMEbus interrupts, VMEbus ACFAIL\* being asserted, VMEbus SYSFAIL\* being asserted, and various internal conditions and errors.

## Chapter 3 – Hardware Description

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Of the eight Universe IIB LINT7# - LINT0# outputs, LINT0# is routed to the PIIX4 PIRQB# input, LINT1# is routed to the PIIX4 EXTSMI# input, and LINT#[7:2] are pulled up via 8.2K resistors.

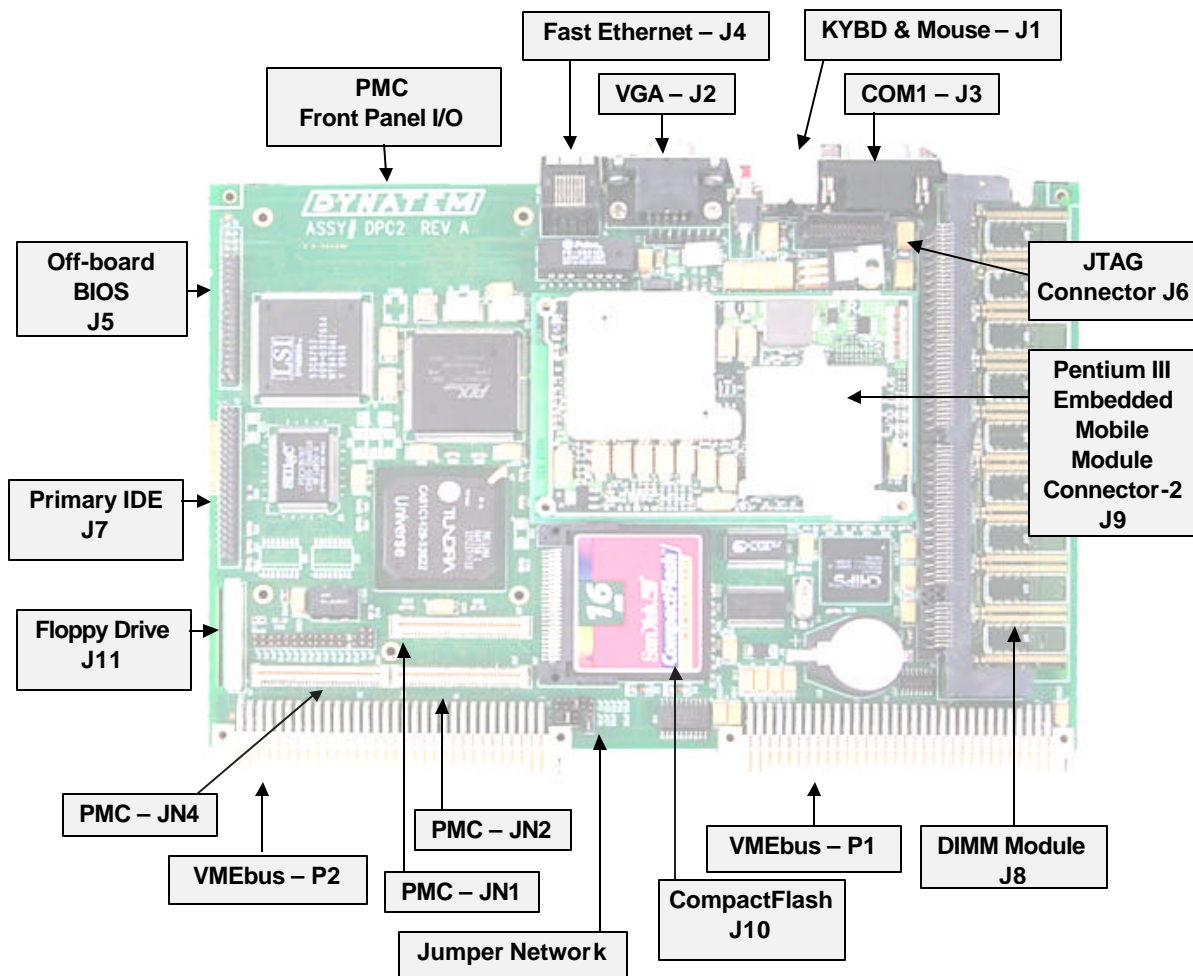
For further details on interrupts, refer to Section 3.9 on the PCI Mezzanine Card (PMC) Slot.

## 4. Installation

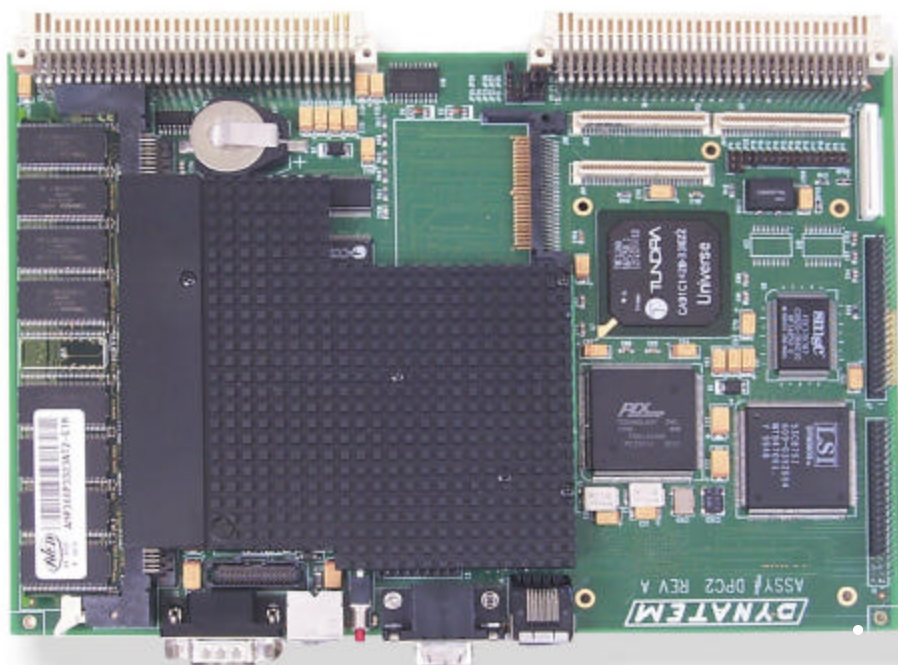
The following sections cover the steps necessary to configure the DPC2 and install it into a VMEbus system for single-slot operation. This chapter should be read in its entirety before proceeding with the installation.

This chapter does not discuss the installation of the DPC2 with the optional DxCI1TB Transition Board or the connection of peripherals accessible via the DxCI1TB (primary IDE, floppy drive, Ultra Wide SCSI, COM2, LPT1, and PC speaker). For information on installing the DPC2 with the DxCI1TB Transition Board, refer to *DxCI1TB Transition Board User's Manual*, available from Dynatem.

The diagram below shows the DPC2 with no PCI Mezzanine Card (PMC). The sections and connectors of the DPC2 referred to in this chapter are pointed out. The connectors that do not go to the front panel have their pin 1 location labeled. The off-board BIOS connector is for factory use.



The diagram above shows the DPC2 with a DIMM memory module and CompactFlash Drive installed.

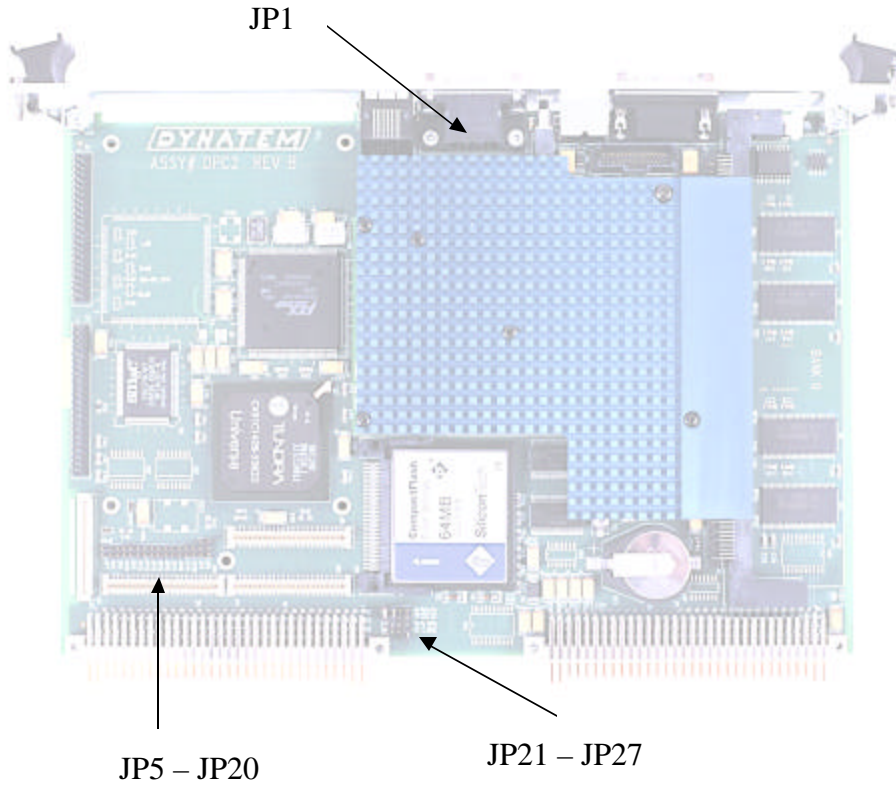


The DPC2 is shipped in an antistatic bag. Be sure to observe proper handling procedures during the configuration and installation process, to avoid damage due to electrostatic discharge (ESD).

The DPC2 uses a heavy heat sink for cooling the EMC-2 Low Power Module (LPM). The LPM has its own heat sink that draws heat off of the Pentium III and the BX Northbridge device. This heat sink in turn is mechanically attached to the black heat sink that can be seen in the photo above. Thermal paste is used to maximize conduction. This heat sink also cools the 5 VDC/3.3 VDC converter. The heat sink was designed to allow replacement of CompactFlash drives and lithium coin cell batteries and to make the connector for the JTAG debug port accessible.

### 4.1 Jumper Selectable Options

The DPC2 contains nine jumpers that the user should be familiar with. These jumpers are shown in the drawing below:



JP1, located beneath the heat sink, is simply used to program an on-board logic device and is of no interest to the user. JP5 through JP16 will route the floppy controller's interface signals to the outer rows of the VMEbus P2 connector. This is an option that is not on the standard board. The following table summarizes all of the on-board jumpers.

With three-pin jumpers, a square pad on the solder side of board identifies pin 1 and it will be closer to the VMEbus backplane than the front panel.

Factory Set Jumpers	Description
JP1	Lattice ISP Connector
<i>JP2</i>	The LED control line for the IDE port will be routed to connector P2 pin C14 (SCZLED#) when closed, for routing IDE to P2 when on-board SCSI isn't used.
<i>JP3</i>	A20 on BIOS Flash U34 (1 & 2 grounds A20, 2 & 3 (default) is GPO27 from the PIIX4 and pulled high). Pin 3 is labeled in the silkscreen.
JP4	BIOS Flash U34 is write protected when pins 2 & 3 are shunted, BIOS can be reprogrammed when pins 1 & 2 are shunted.
JP5	To route Floppy Disk line -INDEX to P2.Z31 instead of PMC I/O
JP6	To route FDC line -DRVS0 to P2.D30 instead of PMC I/O
JP7	To route FDC line -DSKCHG to P2.Z29 instead of PMC I/O
JP8	To route FDC line -MOTR0 to P2.D29 instead of PMC I/O
JP9	To route FDC line -DIR to P2.D28 instead of PMC I/O
JP10	To route FDC line -STEP to P2.Z27 instead of PMC I/O
JP11	To route FDC line -WDATA to P2.D27 instead of PMC I/O
JP12	To route FDC line -WGATE to P2.D26 instead of PMC I/O
JP13	To route FDC line -TRK0 to P2.Z25 instead of PMC I/O
JP14	To route FDC line -WPT to P2.D25 instead of PMC I/O
JP15	To route FDC line -RDATA to P2.D24 instead of PMC I/O
JP16	To route FDC line -HSEL to P2.Z23 instead of PMC I/O
JP21	Closed when there is no Universe IIB on the board
JP26	Enables spread spectrum clocking when closed (default: open)
<i>JP28</i>	Universe drives SYSRESET to VMEbus when closed; strapped closed
<i>JP29</i> (before Rev D)	Put a 4.7 K resistor between pins 2 & 3 when there is on-board SDRAM; put a 0 ohm resistor between pins 1 & 2 if no SDRAM on-board.
<i>JP29</i> (after Rev D)	Slows CPU to 333 MHz when closed for cooler operation (introduced on Rev D)
SW1	Route Chip Enable to on-board BIOS Flash U34
SW2	A software option bit to GPI21 (low (0) when closed)
User Jumpers	Description
JP19	PMCINTB# goes to IRQ7 (1 & 2) or to PIRQA# (2 & 3)
JP20	PMCINTC# goes to IRQ7 (1 & 2) or to PIRQD# (2 & 3)
JP17	Turn off SCSI terminators when closed
JP18	PMCINTC# goes to PIRQB# when closed
JP22	Shunt to put COM1 in RS-232 mode; in RS-422 mode when open
JP23	Universe gets VMEbus SYSRESET when closed
JP24	VMEbus Slot 1 Controller when open
JP25	Shunt to put COM2 in RS-232 mode; in RS-422 mode when open
JP27	For Battery Backed RTC/NVRAM. Normal: 1 & 2, to clear: 2 & 3

*Italicized jumpers have 0805 surface mount pads so they require 0 ohm resistors w/0805 footprints for closing.*

See Section 3.9 for information on jumpers JP18, JP19, and JP20.

JP17 configures terminators for the SCSI interface, as shown below:

SCSI Interface	JP17
On-board terminators enabled	Open
On-board terminators disabled	Closed

**SCSI Termination**

Both COM1 and COM2 can be configured for RS-232 or RS-422/485 operation. Jumpers JP22 and JP25 determine the communication mode of serial ports COM1 and COM2, respectively. See Appendix A for the pin-outs of these two ports.

Communication Mode	JP22	JP25
COM1 RS-232	Closed	
COM1 RS-422/485	Open	
COM2 RS-232		Closed
COM2 RS-422/485		Open

**Communication Mode Selection**

When a VMEbus module occupies slot 1 of the VMEbus chassis (the slot to the extreme left), it must behave as system controller (act as multiprocessing arbiter and generate utility bus signals). Jumper JP24 configures the VMEbus System Controller functionality of the Universe IIB, as shown below:

VMEbus System Controller	JP24
Enabled	Open
Disabled	Closed

**VMEbus System Controller Configuration**

Jumper JP23 lets VMEbus SYSRESETs reset the DPC2 when closed. When open, VMEbus SYSRESETs from other modules will not impact the DPC2.

VMEbus SYSRESET In Selection	JP23
DPC2 Won't Receive SYSRESET's from the VMEbus	Open
DPC2 Receives SYSRESET's from the VMEbus	Closed

**VMEbus SYSRESET In Selection**

Jumper JP28 lets DPC2 SYSRESETs reset the VMEbus when closed. When open, the DPC2 cannot drive SYSRESETs to other modules on the VMEbus. JP28 is strapped closed on the printed circuit board so it must be opened if SYSRESET is not to be driven to the VMEbus (SYSRESET is only driven by the Universe IIB when the DPC2 is a Slot 1 Controller). To reconnect JP28, a 0 ohm resistor w/0805 footprint must be added. JP28 is on the solder (under) side of the DPC2 near the P1 connector.

VMEbus SYSRESET Out Selection	JP28
DPC2 Won't Drive SYSRESETs to the VMEbus	Open
DPC2 Drives SYSRESETs to the VMEbus	Closed

**VMEbus SYSRESET Out Selection**

Jumper JP27 is provided for wiping out the NVRAM. If BIOS parameters are modified and the DPC2 goes into a failure mode, default variables can be restored by grounding the battery supply voltage going to the NVRAM and the RTC. This is done by momentarily shunting pins 2 & 3 of JP27 when power is off. When JP27 is shunted between pins 1 & 2, the RTC and the NVRAM draw supply voltage from the lithium coin cell on-board, from the 5VSTDBY on VMEbus connector P1, or from pin C13 of the P2 VMEbus connector - whichever is highest.

<b>NVRAM / RTC Battery Source</b>	<b>JP27</b>
Draw Battery Voltage from On-board Coin Cell or the VMEbus' 5VSTDBY or Connector P2 Pin C13	1-2
Clear NVRAM & RTC (While Powered Down)	2-3

**Battery Voltage Supply Selection**

### 4.2 CompactFlash Drive Installation

The DPC2 supports a bootable CompactFlash Drive for booting into an Operating System (OS) while occupying only one slot in the VMEbus chassis. Secondary IDE connector J10 is a Type II CompactFlash connector and is used for this purpose. The heat sink for the LPM has a cutaway so that the Flash Drive can be installed and replaced without too much bother.

### 4.3 PCI Mezzanine Card (PMC) Installation

The DPC2 supports a single-width 32-bit PCI Mezzanine Card (PMC) via connectors JN1 and JN2. A JN4 connector is provided for routing I/O from the PMC module to the outer rows (d & z) of a 5-row VMEbus P2 connector. The DPC2 does not contain a JN3 connector for 64-bit PCI support, but cards containing a PN3 connector are accommodated (i.e., no components on the DPC2 interfere with a PMC PN3 connector). To install a PCI Mezzanine Card, follow these steps:

1. Place the DPC2 on a flat surface with the VMEbus connectors towards you and the front panel away from you.
2. Insert the front panel of the PMC board through the DPC2 front panel opening, while keeping the PMC board at a slight angle to the DPC2. This step may require some experimentation due to the EMC gasket on the PMC board that fits snugly between the PMC board front panel and the DPC2 front panel.
3. Line up the PN1/PN2/PN4 connectors on the PMC board with the JN1/JN2/JN4 connectors on the DPC2, and gently press the PMC board into place so that the connectors mate.
4. Install the four mounting screws and washers into the PMC board mounting holes from the bottom side of the DPC2.

#### **4.4 VMEbus Chassis Installation**

Unless your VMEbus chassis features automatic daisy chaining, it will have a set of five jumpers for each slot:

- **Interrupt Acknowledge** – IACKIN\* and IACKOUT\*
- **Bus Grant 0** – BG0IN\* and BG0OUT\*
- **Bus Grant 1** – BG1IN\* and BG1OUT\*
- **Bus Grant 2** – BG2IN\* and BG2OUT\*
- **Bus Grant 3** – BG3IN\* and BG3OUT\*

These jumpers are typically found between slots, and when configuring a VMEbus chassis, care must be taken to correctly determine the slot affected by the jumpers (the slot to the right of the jumpers). The interrupt acknowledge is a daisy chain from the board acknowledging the interrupt request to the boards that can issue an interrupt request. The bus grant signals are daisy chains from the system controller, which contains the bus arbiter, to the boards that can request the bus.

Empty VMEbus slots between boards should have all of these jumpers installed. Any slot containing the DPC2 should have all of these jumpers removed. Any VMEbus slots after the last board in the chassis (that is, the board farthest away from the system controller, which is always in slot 1) do not require these jumpers. For other boards in the VMEbus chassis, refer to their installation instructions for their jumper requirements.

Once the VMEbus chassis jumpers are installed, insert the DPC2 into its designated slot. With the DPC2 ejector handles inward, firmly push the DPC2 into the VMEbus connectors on the chassis. Tighten the screws to the outside of the ejector handles to complete the installation of the DPC2 in the VMEbus chassis.

#### **4.5 Front Panel Connections**

The DPC2 offers front panel connections for COM1, a single connector for PS/2 style keyboard and mouse which requires a “Y” splitter cable, VGA output, 10BaseT/100BaseTX Ethernet, and PMC front panel I/O.

Install all front panel cables by inserting them into the appropriate connector. COM1 and VGA cables can be secured to the DPC2 by tightening their thumbscrews into the connectors’ jackscrews. Mounting hardware for the front panel connectors are isolated from the DPC2’s digital ground. They are continuous with the front panel itself that, in turn, is intended to be common with chassis ground.

#### **4.6 Front Panel Reset Switch and LEDs**

The DPC2 contains a recessed reset switch, accessible from the front panel. To reset the DPC2, press the reset switch using a small screwdriver blade or similar object.

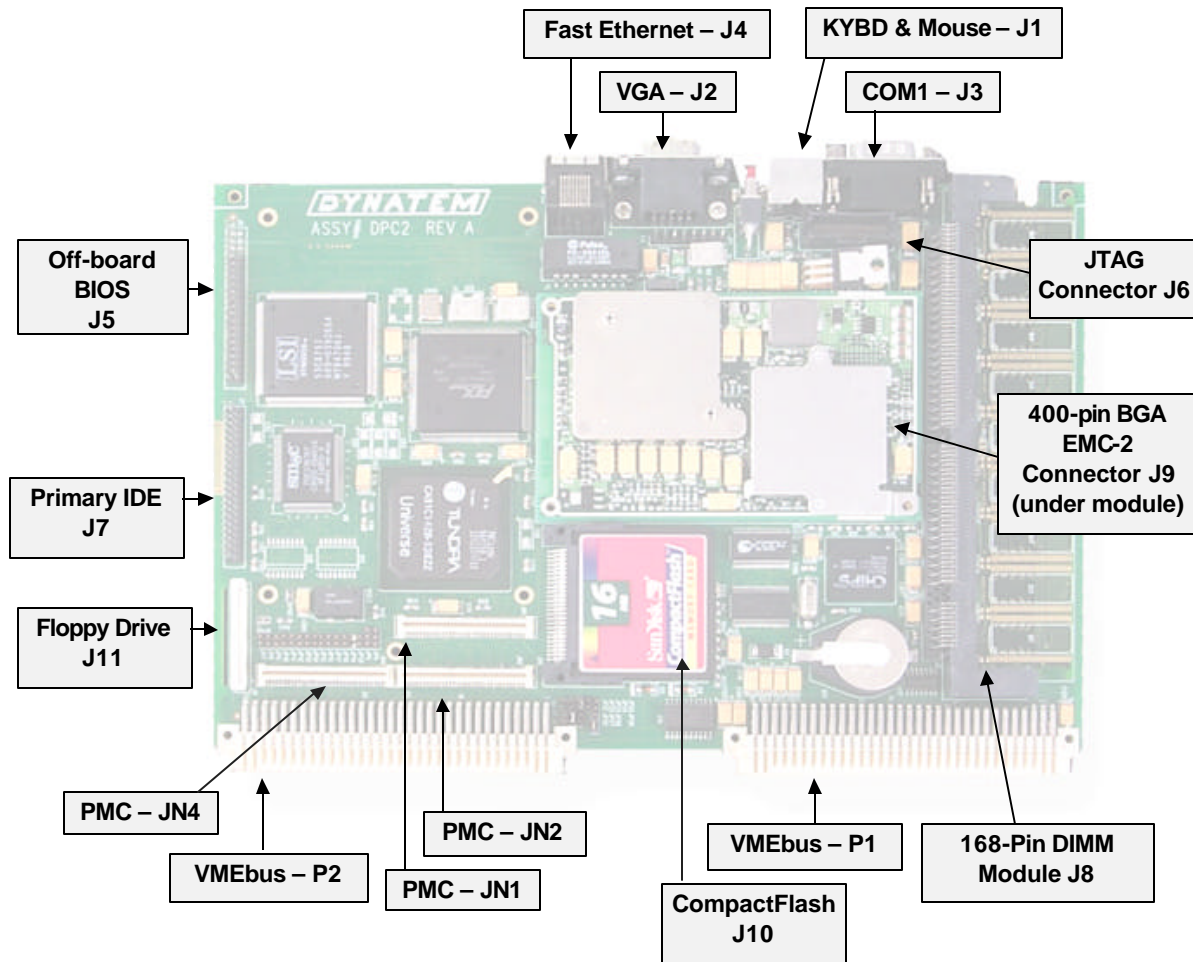
The DPC2 contains three front panel LEDs, which can be viewed through 3 tiny holes in the front panel, located to the left of the reset switch while viewing the DPC2 after it has been installed in the chassis. From top to bottom they are:

- **Link** – Ethernet link is established when on. Labeled CR3.
- **Activity** – Ethernet data is being transmitted or received by the DPC2 when on. Labeled CR2.
- **Speed** – Ethernet data is transferred at 100BaseTX rates when on. Labeled CR1.



## A. Connector Pin-outs

The locations of the DPC2 connectors are shown below. The connectors that do not go to the front panel have their pin 1 location designated accordingly.



## Appendix A - Connector Pin-outs

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### A.1 PS/2 Keyboard/Mouse Connector (J1)

Pin	Signal Description
1	Keyboard Data
2	Mouse Data
3	GND
4	+5 VDC (via 1 amp self-resetting fuse F1)
5	Keyboard Clock
6	Mouse Clock

**Keyboard/Mouse Connector (J1) – Front Panel Mini-DIN Receptacle. The metal shell of the connector goes to chassis ground.**

### A.2 JTAG Debug Port (J6)

This JTAG debug connector permits in-circuit emulation for system debugging.

Pin	Signal	Pin	Signal
1	RESET#	2	GND
3	DBRESET#	4	GND
5	TCX	6	GND
7	TMS	8	TDI
9	POWERON	10	TDO
11	DBINST#	12	TRST#
13	GND	14	BSEN#
15	GND	16	PREQ0#
17	GND	18	PRDY0#
19	GND	20	PREQ1#
21	GND	22	PRDY1#
23	GND	24	PREQ2#
25	GND	26	PRDY2#
27	GND	28	PREQ3#
29	BCLK	30	PRDY3#

**JTAG Connector (J6)**

**A.3 10BaseT/100BaseTX Fast Ethernet Connector (J4)**

Pin	Signal Description
1	Transmit Data + (TX+)
2	Transmit Data - (TX-)
3	Receive Data + (RX+)
4	Transmit Center Tap 1 (CTTX1)
5	Transmit Center Tap 2 (CTTX2)
6	Receive Data - (RX-)
7	Receive Center Tap 1 (CTRX1)
8	Receive Center Tap 2 (CTRX2)

**10BaseT/100BaseTX Fast Ethernet Connector (J4) – Front Panel RJ-45 Connector. The metal shell of the connector goes to chassis ground.**

**A.4 VGA Connector (J2)**

Pin	Signal Description
1	Red Output
2	Green Output
3	Blue Output
4	No connection
5	HSYNC/VSYNC Return (GND)
6	Red Return (GND)
7	Green Return (GND)
8	Blue Return (GND)
9	+5 VDC
10	HSYNC/VSYNC Return (GND)
11	No connection
12	DDCDAT
13	Horizontal Sync (HSYNC) Output
14	Vertical Sync (VSYNC) Output
15	DDCCLK

**VGA Connector (J2) – Front Panel DB15F Connector. The metal shell of the connector goes to chassis ground.**

## Appendix A - Connector Pin-outs

### A.5 COM1 Connector (J3)

See Section 4.1 for instructions on how to determine RS-232 vs. RS-4xx through proper configuration of jumper JP22.

Pin	RS-232 Signals (JP22 Shunted)	RS-4xx Signals
1	Data Carrier Detect (DCD) Input	-TxD
2	Received Data (RxD) Input	-RTS
3	Transmitted Data (TxD) Output	+CTS
4	Data Terminal Ready (DTR) Output	+RxD
5	GND	GND
6	Data Set Ready (DSR) Input	+TxD
7	Request To Send (RTS) Output	+RTS
8	Clear To Send (CTS) Input	-CTS
9	Ring Indicator (RI) Input	-RxD

**COM1 Connector (J3) – Front Panel DB9M Connector. The metal shell of the connector goes to chassis ground.**

### A.6 Primary IDE Interface Connector (J7)

Pin	Signal	Pin	Signal
1	RST#	2	GND
3	D7	4	D8
5	D6	6	D9
7	D5	8	D10
9	D4	10	D11
11	D3	12	D12
13	D2	14	D13
15	D1	16	D14
17	D0	18	D15
19	GND	20	No connection
21	DMARQ0	22	GND
23	IOW#	24	GND
25	IOR#	26	GND
27	IORDY	28	470-ohm pull-down
29	DMAACK0	30	GND
31	IRQ14	32	No connection
33	DA1	34	No connection
35	DA0	36	DA2
37	CS1Fx	38	CS3Fx
39	LED Control	40	GND
41	+5 VDC	42	+5 VDC
43	GND	44	No connection

**Primary IDE Interface Connector (J7) – 44-pin Dual-row 2-mm Header**

**A.7 CompactFlash Interface Connector (J10)**

Pin	Signal	Pin	Signal
1	GND	26	CMPFLASHDET
2	D3	27	D11
3	D4	28	D12
4	D5	29	D13
5	D6	30	D14
6	D7	31	D15
7	CS1#	32	CS3#
8	GND	33	No connection
9	GND	34	DIOR#
10	GND	35	DIOW#
11	GND	36	+5 VDC
12	GND	37	DIRQ
13	+5 VDC	38	+5 VDC
14	GND	39	GND (master)
15	GND	40	No connection
16	GND	41	IDERESET
17	GND	42	DIORDY
18	DA2	43	No connection
19	DA1	44	+5 VDC
20	DA0	45	DASP#
21	D0	46	Pull-up to +5 VDC
22	D1	47	D8
23	D2	48	D9
24	IOCS16#	49	D10
25	No connection	50	GND

**CompactFlash Type II Interface Connector (J10)**

## Appendix A - Connector Pin-outs

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### A.8 Floppy Drive Interface Connector (J11)

For details on the Floppy Drive Interface signals, refer to the *FDC37B78x Manual*.

Pin	Signal Description
1	+5 VDC
2	INDEX#
3	+5 VDC
4	DS0#
5	+5 VDC
6	DSKCHG#
7	No connection
8	No connection
9	No connection
10	MTR0#
11	No connection
12	DIR#
13	No connection
14	STEP#
15	GND
16	WDATA#
17	GND
18	WGATE#
19	GND
20	TRK0#
21	GND
22	WRTPRT#
23	GND
24	RDATA#
25	GND
26	HDSEL#

**Floppy Drive Interface Connector (J11) – 1.00mm ZIF Flex Circuit Connector**

A.9 PCI Mezzanine Card (PMC) Connectors (JN1 and JN2)

Pin	Signal	Pin	Signal
1	5.6K pull-down	2	-12 VDC
3	GND	4	IRQD
5	IRQ (JP19-2)	6	IRQ (JP20-2)
7	No connection	8	+5 VDC
9	IRQD	10	No connection
11	GND	12	No connection
13	PCI CLK	14	GND
15	GND	16	PCI GNT3#
17	PCI REQ3#	18	+5 VDC
19	+5 VDC	20	AD31
21	AD28	22	AD27
23	AD25	24	GND
25	GND	26	C/BE3#
27	AD22	28	AD21
29	AD19	30	+5 VDC
31	+5 VDC	32	AD17
33	FRAME#	34	GND
35	GND	36	IRDY#
37	DEVSEL#	38	+5 VDC
39	GND	40	LOCK#
41	SDONE	42	SBO
43	PAR	44	GND
45	+5 VDC	46	AD15
47	AD12	48	AD11
49	AD9	50	+5 VDC
51	GND	52	C/BE0#
53	AD6	54	AD5
55	AD4	56	GND
57	+5 VDC	58	AD3
59	AD2	60	AD1
61	AD0	62	+5 VDC
63	GND	64	REQ64 (2.7K pull-up)

PCI Mezzanine Card (PMC) Connector (JN1) – Molex 52763-0649

## Appendix A - Connector Pin-outs

Pin	Signal	Pin	Signal
1	+12 VDC	2	TRST (pulled down)
3	TMS (pulled up)	4	No connection
5	TDI (pulled up)	6	GND
7	GND	8	No connection
9	No connection	10	No connection
11	+5 VDC	12	+3.3 VDC
13	PCI RST#	14	GND
15	+3.3 VDC	16	GND
17	No connection	18	GND
19	AD30	20	AD29
21	GND	22	AD26
23	AD24	24	+3.3 VDC
25	AD26 (IDSEL)	26	AD23
27	+3.3 VDC	28	AD20
29	AD18	30	GND
31	AD16	32	C/BE2#
33	GND	34	No connection
35	TRDY#	36	+3.3 VDC
37	GND	38	STOP#
39	PERR#	40	GND
41	+3.3 VDC	42	SERR#
43	C/BE1#	44	GND
45	AD14	46	AD13
47	GND	48	AD10
49	AD8	50	+3.3 VDC
51	AD7	52	No connection
53	+3.3 VDC	54	No connection
55	No connection	56	GND
57	No connection	58	No connection
59	GND	60	No connection
61	ACK64 (2.7K pull-up)	62	+3.3 VDC
63	GND	64	No connection

### PCI Mezzanine Card (PMC) Connector (JN2) – Molex 52763-0649

Note: PMC Connector JN4 is strictly for I/O routing so there is no defined pin-out assignment. Section A.10, on the following pages, shows how the JN4 lines are routed to the outer rows of VMEbus connector P2 (some of these lines are shared with an optional FDC routing to P2).

A.10 VMEbus Connectors (P1 and P2)

Pin	Signal	Pin	Signal	Pin	Signal
A01	D00	B01	BBSY*	C01	D08
A02	D01	B02	BCLR*	C02	D09
A03	D02	B03	ACFAIL*	C03	D10
A04	D03	B04	BG0IN*	C04	D11
A05	D04	B05	BG0OUT*	C05	D12
A06	D05	B06	BG1IN*	C06	D13
A07	D06	B07	BG1OUT*	C07	D14
A08	D07	B08	BG2IN*	C08	D15
A09	GND	B09	BG2OUT*	C09	GND
A10	SYSCLK	B10	BG3IN*	C10	SYSFAIL*
A11	GND	B11	BG3OUT*	C11	BERR*
A12	DS1*	B12	BR0*	C12	SYSRESET*
A13	DS0*	B13	BR1*	C13	LWORD*
A14	WRITE*	B14	BR2*	C14	AM5
A15	GND	B15	BR3*	C15	A23
A16	DTACK*	B16	AM0	C16	A22
A17	GND	B17	AM1	C17	A21
A18	AS*	B18	AM2	C18	A20
A19	GND	B19	AM3	C19	A19
A20	IACK*	B20	GND	C20	A18
A21	IACKIN*	B21	No connection	C21	A17
A22	IACKOUT*	B22	No connection	C22	A16
A23	AM4	B23	GND	C23	A15
A24	A07	B24	IRQ7*	C24	A14
A25	A06	B25	IRQ6*	C25	A13
A26	A05	B26	IRQ5*	C26	A12
A27	A04	B27	IRQ4*	C27	A11
A28	A03	B28	IRQ3*	C28	A10
A29	A02	B29	IRQ2*	C29	A09
A30	A01	B30	IRQ1*	C30	A08
A31	-12 VDC	B31	+5 VDC Standby	C31	+12 VDC
A32	+5 VDC	B32	+5 VDC	C32	+5 VDC

VMEbus Connector (P1) – DIN 41612 96-pin (3 rows x 32 pins)

## Appendix A - Connector Pin-outs

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
Z01	JN4-pin2	A01	SCSI D12#	B01	+5 VDC	C01	COM2 TxD/+CTS*	D01	JN4-pin1
Z02	GND	A02	SCSI D13#	B02	GND	C02	COM2 RxD/-RTS*	D02	JN4-3
Z03	JN4-5	A03	SCSI D14#	B03	No Connect	C03	COM2 RTS/+RTS*	D03	JN4-4
Z04	GND	A04	SCSI D15#	B04	A24	C04	COM2 CTS/-CTS*	D04	JN4-6
Z05	JN4-8	A05	SCSI DPH#	B05	A25	C05	COM2 DTR/+RxD*	D05	JN4-7
Z06	GND	A06	SCSI D0#	B06	A26	C06	COM2 DSR/+TxD*	D06	JN4-9
Z07	JN4-11	A07	SCSI D1#	B07	A27	C07	COM2 DCD/-TxD*	D07	JN4-10
Z08	GND	A08	SCSI D2#	B08	A28	C08	COM2 RI/-RxD*	D08	JN4-12
Z09	JN4-14	A09	SCSI D3#	B09	A29	C09	JN4-28	D09	JN4-13
Z10	GND	A10	SCSI D4#	B10	A30	C10	Speaker Output	D10	JN4-15
Z11	JN4-17	A11	SCSI D5#	B11	A31	C11	+5 VDC	D11	JN4-16
Z12	GND	A12	SCSI D6#	B12	GND	C12	GND	D12	JN4-18
Z13	JN4-20	A13	SCSI D7#	B13	+5 VDC	C13	RTC Battery In	D13	JN4-19
Z14	GND	A14	SCSI DPL#	B14	D16	C14	SCSI LED#	D14	JN4-21
Z15	JN4-23	A15	GND	B15	D17	C15	JN4-30	D15	JN4-22
Z16	GND	A16	SCSI Power**	B16	D18	C16	LPT1 STROBE#	D16	JN4-24
Z17	JN4-26	A17	SCSI Power**	B17	D19	C17	LPT1 AUTOFD#	D17	JN4-25
Z18	GND	A18	IDESPARE***	B18	D20	C18	LPT1 PD0	D18	JN4-27
Z19	JN4-29	A19	SCSI ATN#	B19	D21	C19	LPT1 ERR#	D19	JN4-28
Z20	GND	A20	GND	B20	D22	C20	LPT1 PD1	D20	JN4-30
Z21	JN4-32	A21	SCSI BSY#	B21	D23	C21	LPT1 INIT#	D21	JN4-31
Z22	GND	A22	SCSI ACK#	B22	GND	C22	LPT1 PD2	D22	JN4-33
Z23	JN4-35	A23	SCSI RESET#	B23	D24	C23	LPT1 SLCTIN#	D23	JN4-34
Z24	GND	A24	SCSI MSG#	B24	D25	C24	LPT1 PD3	D24	JN4-36
Z25	JN4-38	A25	SCSI SEL#	B25	D26	C25	LPT1 PD4	D25	JN4-37
Z26	GND	A26	SCSI CD#	B26	D27	C26	LPT1 PD5	D26	JN4-39
Z27	JN4-41	A27	SCSI REQ#	B27	D28	C27	LPT1 PD6	D27	JN4-40
Z28	GND	A28	SCSI IO#	B28	D29	C28	LPT1 PD7	D28	JN4-42
Z29	JN4-44	A29	SCSI D8#	B29	D30	C29	LPT1 ACK#	D29	JN4-43
Z30	GND	A30	SCSI D9#	B30	D31	C30	LPT1 BUSY#	D30	JN4-45
Z31	JN4-46	A31	SCSI D10#	B31	GND	C31	LPT1 PE	D31	GND
Z32	GND	A32	SCSI D11#	B32	+5 VDC	C32	LPT1 SLCT	D32	+5 VDC

### VMEbus Connector (P2) – DIN 41612 160-pin (5 rows x 32 pins)

JN4 is the PMC general purpose I/O connector.

\* COM2 Differential RS-422/485 signals are distinguished from RS-232 signals by the “+” or “-” signs before their labels. COM2 is in the RS-232 mode when jumper JP25 is shunted.

\*\* SCSI termination power (pins A16 and A17) is supplied via a 1 amp self-resetting fuse (F5).

\*\*\*IDESPARE was Ground on the DRC1 but it is now needed to route IDE DD15 when IDE is routed to P2 – see the next page.

## Appendix A – Connector Pin-outs

If SCSI is not supported on the DPC2, the primary IDE interface can be routed out to P2, row A. In order to do this, 0 ohm resistor networks RP3, RP7, RP12, RP18, RP25, RP30, and RP31 must be populated. These networks are located on the DPC2 where SCSI controller U4 would normally go. This is a non-standard configuration that must be special ordered from Dynatem. In other words, don't do this at home – without permission from Dynatem.

Also, the floppy disk controller (FDC) signals may be routed to rows D & Z of P2 by shunting jumpers JP5 through JP16. ***Be careful that these lines don't overlap with PMC I/O.*** This is also a non-standard mode of operation.

Both P2 IDE and P2 FDC expansion are supported by the DPC2PTB (Rev 3 + for IDE) and the P2 pin-out for these custom configurations are in the table below. FDC signals are in bold and IDE signals are italicized.

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
Z01	JN4-pin2	A01	<i>PDREQ</i>	B01	+5 VDC	C01	COM2 TxD/+CTS*	D01	JN4-pin1
Z02	GND	A02	<i>PDIOW#</i>	B02	GND	C02	COM2 RxD/-RTS*	D02	JN4-3
Z03	JN4-5	A03	<i>PDIOR#</i>	B03	No Connect	C03	COM2 RTS/+RTS*	D03	JN4-4
Z04	GND	A04	<i>PDIORDY</i>	B04	A24	C04	COM2 CTS/-CTS*	D04	JN4-6
Z05	JN4-8	A05	<i>PDDACK#</i>	B05	A25	C05	COM2 DTR/+RxD*	D05	JN4-7
Z06	GND	A06	<i>PDIRQ</i>	B06	A26	C06	COM2 DSR/+TxD*	D06	JN4-9
Z07	JN4-11	A07	<i>PDA1</i>	B07	A27	C07	COM2 DCD/-TxD*	D07	JN4-10
Z08	GND	A08	<i>PDA0</i>	B08	A28	C08	COM2 RI/-RxD*	D08	JN4-12
Z09	JN4-14	A09	<i>PDCS1#</i>	B09	A29	C09	JN4-28	D09	JN4-13
Z10	GND	A10	<i>RSTDRV#</i>	B10	A30	C10	Speaker Output	D10	JN4-15
Z11	JN4-17	A11	<i>PDA2</i>	B11	A31	C11	+5 VDC	D11	JN4-16
Z12	GND	A12	<i>PDCS3#</i>	B12	GND	C12	GND	D12	JN4-18
Z13	JN4-20	A13	<i>PDD7</i>	B13	+5 VDC	C13	RTC Battery In	D13	JN4-19
Z14	GND	A14	<i>PDD6</i>	B14	D16	C14	SCSI LED#	D14	JN4-21
Z15	JN4-23	A15	GND	B15	D17	C15	JN4-30	D15	JN4-22
Z16	GND	A16	Not Used but tied together	B16	D18	C16	LPT1 STROBE#	D16	JN4-24
Z17	JN4-26	A17		B17	D19	C17	LPT1 AUTOFD#	C17	JN4-25
Z18	GND	A18	<i>PDD15***</i>	B18	D20	C18	LPT1 PD0	D18	JN4-27
Z19	JN4-29	A19	<i>PDD5</i>	B19	D21	C19	LPT1 ERR#	D19	JN4-28
Z20	GND	A20	GND	B20	D22	C20	LPT1 PD1	D20	JN4-30
Z21	JN4-32	A21	<i>PDD4</i>	B21	D23	C21	LPT1 INIT#	D21	JN4-31
Z22	GND	A22	<i>PDD3</i>	B22	GND	C22	LPT1 PD2	D22	JN4-33
Z23	<b>Hdsel#</b>	A23	<i>PDD2</i>	B23	D24	C23	LPT1 SLCTIN#	D23	JN4-34
Z24	GND	A24	<i>PDD1</i>	B24	D25	C24	LPT1 PD3	D24	<b>Rdata#</b>
Z25	<b>Trk0#</b>	A25	<i>PDD0</i>	B25	D26	C25	LPT1 PD4	D25	<b>Wpt#</b>
Z26	GND	A26	<i>PDD8</i>	B26	D27	C26	LPT1 PD5	D26	<b>Wgate#</b>
Z27	<b>Step#</b>	A27	<i>PDD9</i>	B27	D28	C27	LPT1 PD6	D27	<b>Wdata#</b>
Z28	GND	A28	<i>PDD10</i>	B28	D29	C28	LPT1 PD7	D28	<b>Dir#</b>
Z29	<b>Dskchg #</b>	A29	<i>PDD11</i>	B29	D30	C29	LPT1 ACK#	D29	<b>Motr0#</b>
Z30	GND	A30	<i>PDD12</i>	B30	D31	C30	LPT1 BUSY	D30	<b>Drvs0#</b>
Z31	<b>Index#</b>	A31	<i>PDD13</i>	B31	GND	C31	LPT1 PE	D31	GND
Z32	GND	A32	<i>PDD14</i>	B32	+5 VDC	C32	LPT1 SLCT	D32	+5 VDC

**VMEbus Connector (P2) with special IDE & FDC signal routing – 160-pin (5 rows x 32 pins)**

## Appendix A - Connector Pin-outs

### A.11 External BIOS and USB Connector Pin-out (J5)

Connector J5 is a 44-pin 2-mm connector similar to the IDE connector J7. J5 is used to route the BIOS interface externally for on-board BIOS programming and debugging. USB interface lines are also routed from the PIIX4 device to pins 1 through 8. Except for the IDE LED line routed to pin 43, all other lines are intended for an off-board BIOS interface (SW1A must be open; this capability is really for in-factory use). The following table shows J5's pin-out.

Pin	Signal	Pin	Signal
1	USB1 Vcc	2	USB0 Vcc
3	USB1-	4	USB0-
5	USB1+	6	USB0+
7	USB1 GND	8	USB0 GND
9	GND	10	GND
11	SA0	12	XD0
13	SA1	14	XD1
15	SA2	16	XD2
17	SA3	18	XD3
19	SA4	20	XD4
21	SA5	22	XD5
23	SA6	24	XD6
25	SA7	26	XD7
27	SA8	28	GND
29	SA9	30	SA18
31	SA10	32	SA17
33	SA11	34	SA16
35	SA12	36	SA15
37	SA13	38	SA14 (redundant)
39	SA14	40	+3.3 VDC
41	MEMW#	42	MEMR#
43	IDE_HD_LED#	44	BIOSCS#

**External BIOS and USB Connector (J5) – 44-pin Dual-row 2-mm Header**

## B. Address Maps, Interrupts, DMA Channels

Tables of the DPC2's address maps, interrupt request assignments, and DMA channel usage are given in the following sections. All addresses are shown in hexadecimal notation.

### B.1 Memory Map

The DPC2's memory map is shown below:

Address Range	Description
00000000 - 0007FFFF	DOS area main memory
00080000 - 0009FFFF	DOS area main or PCI memory
000A0000 - 000BFFFF	Video Buffer
000C0000 - 000FFFFF	BIOS and Expansion Region
00100000 - Top of On-board SDRAM Memory*	DRAM
Top of On-board SDRAM Memory* to 4 GB	PCI Memory Address Range
FEC00000 - FECFFFFFF, FEE00000 - FEEFFFFFF	APIC Configuration Area (unused on DPC2)
FFFE0000 - FFFFFFFF	High BIOS Area

\*Top of Memory depends on how much SDRAM is being used in the DPC2's DIMM module. So it will vary from 128 MB (only on-board SDRAM is used and the DIMM is empty) to 384 MB.

For further details on the DPC2 memory space map, refer to Section 4.1.1 in *Intel's 440BX AGPset – 82443BX Host Bridge/Controller Datasheet*, available from Intel Corporation.

### B.2 PCI/AGP Configuration Space Map

The PCI configuration space map is shown below. The Vendor ID and Device ID in hex for the PMC slot are shown as *xxxx*, since they depend on the type of device installed in the PMC slot.

IDSEL	Bus	Dev	Fcn	VenID	DevID	Description
—	00	00	0	8086	1250	82443BX Host Bridge/Controller
AD18	00	07	0	8086	7110	82371SB (PIIX4) PCI-ISA Bridge
AD18	00	07	1	8086	7111	82371SB PCI-IDE Interface
AD18	00	07	2	8086	7112	82371SB PCI-USB Interface
AD18	00	07	3	8086	7113	82371SB Power Mgmt & DPC2 Watchdog
AD23	00	0C	0	8086	1229	82559 Fast Ethernet Controller
AD24	00	0D	0	1000	000F	SYM53C875 Ultra Wide SCSI Controller
AD26	00	0F	0	xxxx	xxxx	PCI Mezzanine Card (PMC) Slot
AD27	00	10	0	10E3	0000	Universe IIB CA91C142B PCI-VMEbus Interface

## Appendix B – Address Maps, Interrupts, DMA Channels

The 69030 Graphics Controller is the only one AGP device on the DPC2. The AGP configuration space map is shown below:

IDSEL	Bus	Dev	Fcn	VenID	DevID	Description
AD17	01	01	0	102C	0C30	69030 Accelerated Graphics Controller

Note: If an XPMC3 card is used with the DPC2 for PMC expansion, its secondary bus will be Bus 02 because of the interpolation of the AGP bus.

### B.3 Interrupt Request Routing

The ISA interrupt request routing is shown below:

IRQ	Description
0	Timer 0 (PIIX4)
1	Keyboard (FDC37B78x's keyboard/mouse controller)
2	Cascade Interrupt from slave PIC (PIIX4)
3	COM2/COM4 (FDC37B78x)
4	COM1/COM3 (FDC37B78x)
5	LPT2 (FDC37B78x)
6	Floppy Drive (FDC37B78x)
*7	LPT1 (FDC37B78x)
8	Real Time Clock (PIIX4)
9	No connection (pulled up via 8.2K)
10	No connection (pulled up via 8.2K)
11	No connection (pulled up via 8.2K)
12	Mouse (FDC37B78's keyboard/mouse controller)
13	Math Coprocessor (PIIX4)
14	Primary IDE Interface (PIIX4)
15	Secondary IDE Interface (PIIX4, via MIRQ0)

The PCI interrupt request routing to the Intel 82371SB PCI-ISA Bridge (PIIX4) is shown below:

PIIX4 PCI IRQ	Description
PIRQA#	Symbios SYM53C875 IRQ/
*PIRQB#	Tundra Universe IIB CA91C142B LINT0#
PIRQC#	Intel 82559 INTA#
*PIRQD#	PMC Slot INTA#, INTB#, INTC#, INTD#

\*See Section 3.9 for alternate routings from the PMC expansion slot and from Dynatem's XPMC3 3-slot PMC expansion card.

For further details on interrupts, refer to the documentation for the various peripherals that generate interrupts, as well as *Intel 82371AB (PIIX4) – PCI ISA IDE Xcelerator* and *Intel 82371AB (PIIX4) PCI ISA IDE Xcelerator Specification Update*, available from Intel Corporation.

**B.4 ISA DMA Channel Assignments**

The ISA DMA channel assignments are shown below:

DMA Channel	Description
0	Super I/O chip FDC37B78x DMA Channel 0
1	FDC37B78x DMA Channel 1
2	FDC37B78x DMA Channel 2
3	FDC37B78x DMA Channel 3
4	No connection
5	No connection
6	No connection
7	No connection

5.6K resistors pull down all DMA Request lines. For further details on ISA DMA channel usage, refer to *Intel 82371AB (PIIX4) – PCI ISA IDE Xcelerator* and *Intel 82371AB (PIIX4) PCI ISA IDE Xcelerator Specification Update*, available from Intel Corporation, as well as the *FDC37B78x Data Sheet*, available from Standard Microsystems Corporation.

**B.5 PCI Bus Request/Grant Routing**

The PCI bus request/grant routing to the Intel 82443BX System Controller (440BX) is shown below:

TXC REQ#/GNT#	Description
REQ0#/GNT0#	Intel 82559 REQ#/GNT#
REQ1#/GNT1#	Tundra Universe IIB CA91C142B REQ#/GNT#
REQ2#/GNT2#	Symbios SYM53C875 REQ/ GNT/
REQ3#/GNT3#	PMC Slot REQ#/GNT#

For further details on the PCI bus request/grant signals, refer to *Intel 440BX AGPset – 82443BX Host Bridge/Controller Datasheet*, available from Intel Corporation.

### C. Power and Environmental Requirements

The DPC2 power and environmental requirements are shown in the tables below. +/- 12 VDC are routed from the VMEbus connector to the PMC connector but they are not used by the DPC2 itself.

Condition	Power Requirements
500 MHz Pentium III, 256 KB on-die L2 Cache	+5 VDC @ 4.4 A typ. 3.0 VDC Lithium Coin Cell @ 2.4 $\mu$ A

**Power Requirements**

The 3 Volt lithium coin cell is a CR2032 with 190 mAh capacity and it is used to battery-back the Real Time Clock, the 2 MB of NV-SRAM, and the BIOS's NV-RAM. At 2.4  $\mu$ A this battery should last for nine years with power off.

Condition	Environmental Requirements
Operating Temperature	-40° to +85° C
Storage Temperature	-50° to +105° C

**Environmental Requirements**