



The CPD2 is a form/fit/function upgrade to the CPD shown above with XPDRIO

## CPD2

The CPD2 is a 6U single-slot Compact PCI (PICMG 2.16 compatible) platform based on the Intel® Core™2 Duo Mobile Processor L7400 at 1.5 GHz or the T7400 at 2.16 GHz. The CPD2 takes advantage of the Core2-Duo's low 17 W power consumption (at 1.5 GHz) as a rugged Single Board Computer (SBC) and it is optionally available as a conduction-cooled Compact PCI module with wedge locks and a full-board heat sink for high shock/vibration environments and temperature extremes. For the conduction-cooled version, see CRD2.

### Changes from the CPD

The CPD2 is a form/fit/function replacement to the CPD. While all I/O interfaces are unchanged, the redesign addressed a few key issues to improve performance of the CPD as follows:

Each PMC module now interfaces directly to the E7520 MCH via a Tsi384 PCIe to PCI-X bridge. By converting x4 PCI Express to PCI-X at 64-bit and 133MHz, each PMC can now realize a maximum bandwidth of 1 GB/sec. The CPD had both PMC cards routed from the 6300 I/O controller hub. By routing PMC modules directly to the E7520, the CPD2 offers much greater bandwidth between PMC and processor and PMC and memory. This change takes advantage of higher performance PMC modules. The XMC interface continues to be x8 PCI Express direct from the E7520. These changes will have no impact on application software already developed for the CPD.

A second change from the CPD is the elimination of CompactFlash and its replacement with 16 GB of soldered NAND Flash. This makes the CPD2 more rugged, and provides higher performance Flash at less cost.

### **Core™2 Duo Mobile Processor**

1.5 GHz Or 2.16 GHz, 479-pin uFC-BGA Core 2 Duo manufactured with low-power 65 nm process  
4 MB L2 Cache  
667 MHz front side bus  
64-bit OS and application support

### **Single-slot Operation**

Single-slot CompactPCI operation with 16 GB of on-board Flash disk for bootable mass storage

### **E7520 & 6300ESB Chipset**

Two x4 PCI Express interfaces are routed to two dual Gb Ethernet controllers  
Two x4 PCI Express interfaces are routed to the two PMC sites via two Tsi384 PCIe to PCI-X bridges. This provides each PMC site with a dedicated 64-bit 133 MHz PCI-X bus with a 1 GB bandwidth  
One x8 PCI Express interfaces is routed to an XMC site  
DDR2-400 DRAM interface with a max memory bandwidth of 6.4 GB/second  
Four USB 2.0 Ports  
PATA/100 and SATA/150 support  
PCI-X 64/66 for the PLX PCI6466 PCI/PCI bridge  
PCI 32/33 for SM712 VGA controller

### **DRAM**

2 or 4 GBytes of DDR2-400 memory  
Two banks that are each 64 bits wide with ECC support

### **CompactPCI**

PICMG 2.0 R3.0 Compliant  
PLX non-transparent PCI-PCI bridge provides 64-bit CompactPCI transfer rates at 66 MHz  
Universal bridge lets the CPD2 operate as a system controller or a peripheral slot module  
Supports Hot Swapping according to PICMG 2.1 R2.0  
Connectors J3 and J5 are used for I/O expansion

### **PMC Expansion**

Two PMC sites each with a dedicated 64-bit 133 MHz PCI-X bus interfaced to the E7520 via two separate Tsi384 PCIe to PCI-X bridges. This architecture provides 1 GB access to E7520  
One of PMC sites supports XMC modules with x8 PCIe

### **Ethernet/PICMG 2.16**

Two Intel 82571EB dual PCI express Ethernet controllers provide a total of four 10/100/1000BaseTX ports  
Two ports routed to the front panel  
Two ports routed to the J3 connector in compliance with PICMG 2.16 for backplane fabric switching or for alternate routing to an optional rear I/O card

### **Graphics**

The Silicon Motion SM712 ultra low-power display controller with 4 MB on-chip memory  
VGA routed to J5

### **IDE/Flash**

Primary ATA/100 DMA IDE interface is optionally accessible from the J5  
Secondary IDE port is routed to a Silicon Motion SM-2231 NAND Flash controller.  
16 GB of NAND Flash is installed

### **BIOS**

Phoenix's flash-based system BIOS with boot options including CD-ROM, USB, and PXE over Ethernet

### **Watchdog**

Programmable watchdog timer for system recovery

### **I/O interfaces accessible from the front panel**

Dual 10/100/1000BaseTX, Dual USB 2.0, access to both PMC sites

### **I/O interfaces routed to optional rear plug-in board**

VGA, IDE, COM1/2/3/4 (COM2 optionally RS-422), dual Serial ATA, keyboard, mouse, and dual USB 2.0 ports (routed through J5)  
Two Gb Ethernet ports in compliance with PICMG 2.16 (routed through J3)  
Access to both PMC sites

### **Rear Transition Module**

XPDRIO rear I/O interface board with standard connectors for all I/O routed to rear

### **Operating temperature**

The CPD2 has a standard operating temperature range of 0°/+70° C  
Extended temp versions are available

### **Rugged/Conduction-cooled Versions**

CRD2 is a conduction-cooled version of the CPD2  
Convection-cooled and conduction-cooled versions have conformal coating as an option

### **Net Weight**

Approximately 15 oz

### **Power Requirements**

1.5 GHz L7400: +5VDC @5.5A peak,  
3.3VDC@2.0A steady  
3.0VDC Lithium Coin Cell @3.4 A  
2.16 GHz T7400: +5VDC @8.0A peak



### Core™2 Duo Mobile Processor L7400 or T7400

Delivering breakthrough energy efficient performance for embedded platforms. 65 nm process technology makes it possible to integrate two complete execution cores in one physical package, providing advancements in simultaneous computing for multi-threaded applications and multi-tasking environments. While incorporating advanced technology these CPUs remain software compatible with previous IA-32 processors. Execute four instructions per cycle to improve execution speed and efficiency using 14-stage pipeline. Support 64-bit instructions, providing flexibility for 64-bit and 32-bit applications and operating systems.

### DRAM

The CPD2 supports 2 or 4 GBytes of DRAM and its DDR2-400 memory technology is ideal for memory-intensive applications. The memory subsystem interface to E7520 is dual channel for a total system bandwidth of up to 6.4 GB/second. ECC error correction is supported.

### Chipset

The E7520 Memory Controller Hub (MCH) and 6300ESB I/O Controller Hub (ICH) chipset supports

PCI-X and PCIe expansion, USB 2.0, ATA/100, and Serial ATA (SATA). Two Gb Ethernet ports and two USB 2.0 ports are accessible from the front panel in addition to two PMC bezels. On-board Flash accessible from an IDE port permits single-slot booting. Two PICMG 2.16-compliant, 10/100/1000BaseTX ports are routed to the backplane. Two SATA ports, VGA video, up to four COM ports, an optional IDE interface, PS/2 mouse & keyboard, and two more USB 2.0 ports are routed to the backplane. Two PMC-X sites are provided for additional I/O expansion. One of the sites is XMC compatible and supports x8 PCIexpress. Conventional PC I/O is accessible with industry-standard connectors on optional rear I/O modules.

The Intel® 6300ESB I/O Controller Hub (ICH) supports legacy and more cutting edge I/O. It is designed for use with the MCH. Intel has integrated features into the ICH that offer the performance, stability and reliability customers require for embedded computing applications. It improves bandwidth via PCI-X 64/66 and PCI 32/33 support. It also provides port 60/64 emulation, dual UARTs, four USB 2.0 ports, two SATA ports, primary and secondary IDE, and a two-stage watchdog timer. The Intel 6300ESB ICH and associated drivers help reduce support and validation costs.

#### Ordering Information:

<u>Part#</u>	<u>Description</u>
CPDWRS	CompactPCI single-slot processor with 1.5 GHz Core2-Duo, 2 GB DDR-400. With CompactPCI, PICMG 2.16, IPMI. With 16 GB NAND Flash installed
xxxxSx	Upgrade to 4 GB DDR2-400
xxxxxT	Upgrade to 2.16 GHz Core2 Duo T7400
xxxxxxx-ER	Extended operating temperature
CONCOAT	Conformal coating option
XPDDRIO	Optional rear I/O interface board with: <ul style="list-style-type: none"> <li>• USB connector</li> <li>• 40-pin IDE connector</li> <li>• Two RJ-45 connectors for Gb Ethernet</li> <li>• Two SATA connectors</li> <li>• COM 1,2,3,4 connector (two are MDSM)</li> <li>• PS/2 keyboard mouse</li> </ul>

